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FAULT TREE ANALYSIS OF THE LPTR SCRAM SYSTEM

W. Keith Mortensen
Jack W. Savage

December 13, 1974

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FAULT TREE ANALYSIS OF THE LPTR SCRAM SYSTEM

Abstract

The protective control or scram system of the Livermore Pool Type Reactor (LPTR) has been subjected to fault tree analysis to determine its vulnerability to various component failures or other untoward events both credible and incredible.

This report describes the analysis and discusses the results. The principal result is that no single component failure nor any single credible event can result in a failure of the reactor to scram when a scram is required.

Introduction

The Livermore Pool Type Reactor (LPTR) is a scientific research reactor used primarily as a source of neutrons for irradiation experiments. It is designed to operate at a maximum power level of 3 MW thermal. A detailed description of the reactor and its protection system is given in the LPTR Safety Analysis Report.¹

The staff at LPTR performed the fault tree analysis described here to determine whether the scram system could with-

stand a single failure and still shut down the reactor. As a result of our analysis we conclude that no single component failure nor any single credible event can result in a failure of the reactor to scram when a scram is required.

The appendices to the report include control system diagrams for the LPTR, diagrams of the fault tree analyzed in this study, and results of the computer analysis of the fault tree.

The LPTR Control System

The reactor is brought to its operating power of 3 MW thermal by manually positioning four shim rods to achieve the desired criticality and balance in the reactor core. The power is then automati-

cally regulated by a fifth regulating rod.

Reactor shutdown is accomplished by inserting the four shim rods into the core. Any two shim rods fully entering the core insert sufficient negative reactivity to shut the reactor down.

The shim rods are coupled to the rod drive assemblies by sensitive

1. Safety Analysis Report for the Livermore Pool Type Reactor, Lawrence Livermore Laboratory, Rept. UCRL-51421 (Sept. 18, 1974).

electromagnets. When a magnet is de-energized the associated shim rod falls by force of gravity back into the core. Each magnet is powered by a separate dc power supply and driven by a separate vacuum-tube amplifier. The safety interlock chain (shown on page 24 of the control system drawings, Appendix A) removes the ac power from all four magnet power supplies through the contacts of relay 62.

The magnet amplifiers control the current at the negative terminals of the magnets. The inputs to the four magnet amplifiers are tied to a common bus called the sigma bus. The sigma bus is driven by four independent sigma amplifiers, any one of which will drive the

four magnet amplifiers to cutoff. Three of these sigma amplifiers sense power level, resulting in a scram at a power level of 4.5 MW. The fourth sigma amplifier initiates a scram when the period is less than 1 sec.

The block diagram of reactor nuclear instrumentation is shown in Fig. 1. Figure 2 shows how the sigma bus and associated amplifiers are interconnected.

Included for reference in Appendix A are pages 8, 13, 14, and 24 of Dwg. No. LEA-01-3154-01, the drawings of the control system for the LFTR, which contain the circuits for the safety interlock chain and the associated relay coils.

Fault Tree Analysis of the Control System

Fault tree analysis is a technique by which computers can be used to determine which faults and which combinations of faults can result in a particular system failure. References 2 and 3 discuss the fault tree analysis method in more detail.

In this report the system failure event of interest is: three or more shim rods fail to fully enter the core when a scram condition exists. This is called the "top event."

The analysis is accomplished by drawing a fault tree model which uses a logic symbol format to represent the sensing and control functions of the reactivity control system of the reactor as they relate to the top event. Five symbols make up the fault tree: "and" gates, "or" gates, circles, diamonds, and houses (see Fig. 3).

An "and" gate requires that all inputs to it be satisfied before an output from it will occur.

An "or" gate requires only that one or more of the inputs to it be satisfied before an output from it will occur.

A circle represents a component primary failure, which is sufficient to actuate an input to a gate. The meaning of "component" is subject to definition to suit the case being analyzed, but in all cases it is the final termination of a particular branch of the fault tree, as

2. D. F. Haasli, "Advanced Concepts in Fault Tree Analysis," in System Safety Symposium, June 8-9, 1965 (The Boeing Company, Seattle, Washington, 1965).
3. M. E. Stewart et al., Reliability Analysis of the Power Burst Facility Reactor Protection System, Idaho Nuclear Corporation, Idaho Falls, Idaho (Dec. 1969).

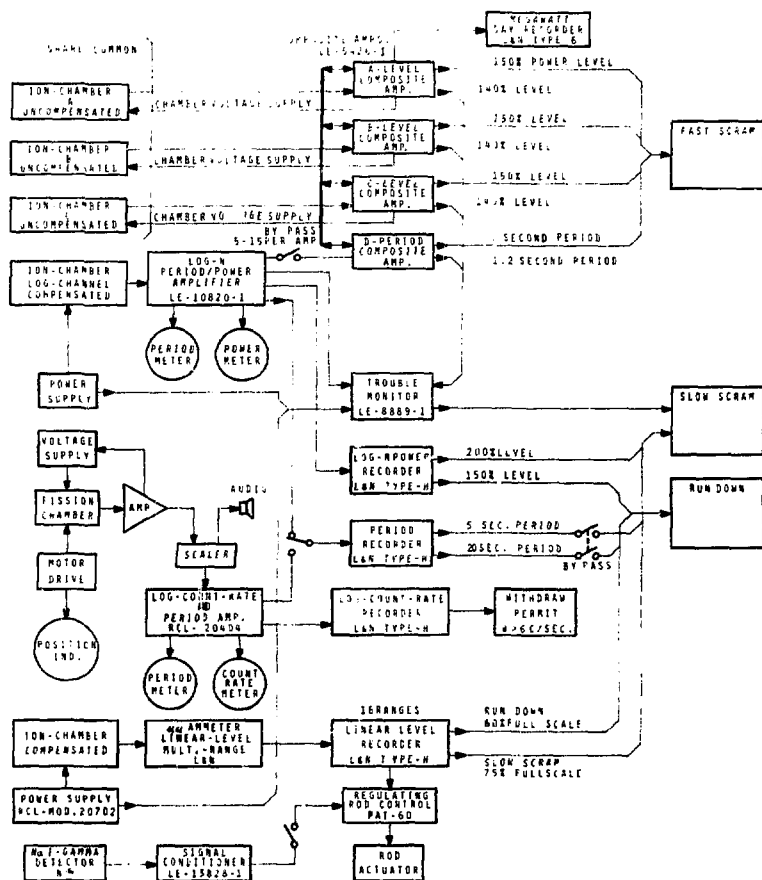


Fig. 1. Block diagram of LPTR nuclear instrumentation.

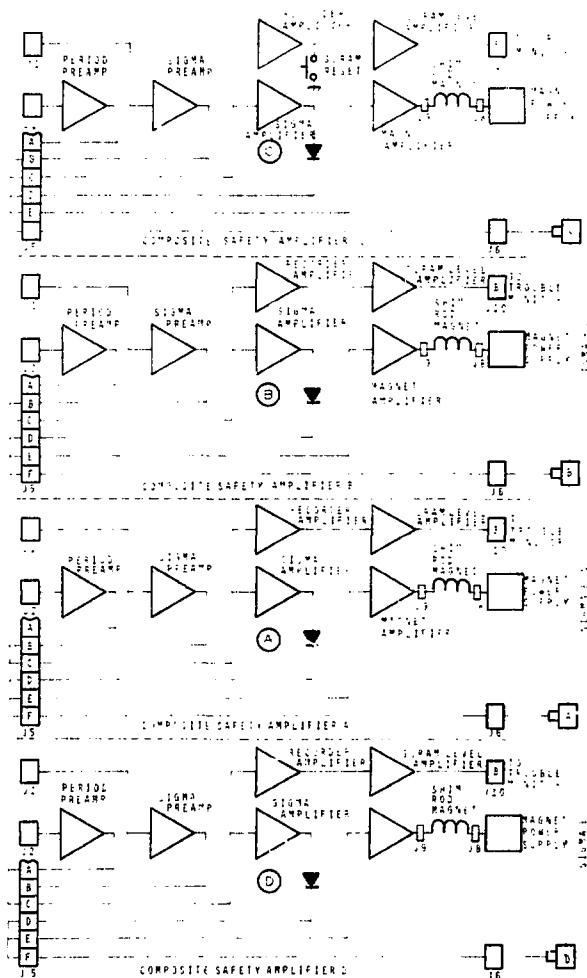


Fig. 2. Interconnection of sigma bus and associated amplifiers.

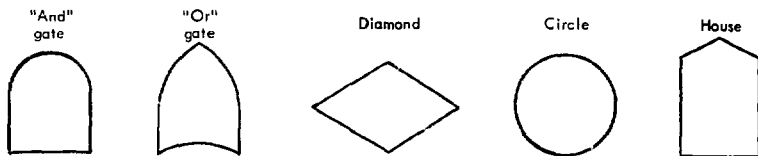


Fig. 3. Symbols used in fault tree analysis.

determined by the desired degree of resolution of the analysis. For example, a circle may represent a single component or even a subcomponent, such as the coil of a relay, while a second circle may represent the contacts. Or one circle may represent the normally open contacts, while another may represent the normally closed contacts. In another case a circle may represent an entire amplifier or even a system consisting of amplifier, detector, and power supply. In general, circles represent components or systems which may fail to perform their intended functions when needed.

A diamond is similar to a circle in that it represents an event which is sufficient to actuate an input to a gate, and is also the termination of a particular branch of the tree. It differs, however, in that it represents a chassis, a sub-system, an open- or short-circuit wiring fault, a circuit discontinuity, a human action, or other event for which the analysis is truncated before there is sufficient detail developed for it to be represented by the additional tree branches which would ultimately end in primary fault circles. The desired degree of resolution dictates when a particular branch can be terminated in a diamond.

Diamonds on the fault tree represent unusual failures or abnormal occurrences.

Examples are a short circuit to a voltage source, operator error, and failures requiring limiting conditions in order to result in a fault. Some diamonds represent events which are considered to be incredible. Each diamond is explained by a numbered diamond note.

Houses in the tree are used as switches to enable or disable portions of the tree, depending upon which scram conditions exist in the analysis being conducted. Each scram condition can be enabled individually, or several may be enabled simultaneously. For example, one may expect that both fast period and high power may exist simultaneously. There are 49 house inputs which serve as switches to enable the various scram conditions.

The fault tree is so constructed that it can represent the scram system for any combination of scram conditions. Table 1 lists each of the possible scram conditions. These may occur singly or in combinations of two or more occurring simultaneously. (Some are mutually exclusive, and some are included automatically as part of another scram condition.) Table 2 lists the house conditions which were included in the rates input portion of the data cards for this study to simulate 17 scram conditions for which computer runs were made.

Table 1. Scram conditions and mechanisms of the LPTR.

Condition causing scram	Mechanism producing scram
<u>Fast scrams</u>	
Power ≥ 4.5 MW	Sigma bus
Period ≤ 1 sec	Sigma bus
<u>Slow scrams</u>	
Power ≥ 6 MW (log N)	RE-85 ^a
Power ≥ 4.2 MW:	
Safety amp A	RE-81
Safety amp B	RE-80
Safety amp C	RE-82
Period ≤ 1.2 sec (safety amp D)	RE-83
Period ≤ 5 sec (period recorder)	RE-84
Power $\geq 75\%$ of linear recorder scale	RE-85
Primary coolant flow low	RE-75
Experiment scram	RE-32
Amplifier or power supply troubles	RE-16, -17, -18, -19 in trouble monitor
Rod drop test	RE-2 in rod drop tester
Pool level low	RE-60
Primary coolant temperature high	RE-2 in primary coolant temperature monitor
Scram button pushed	PB-1 ^b

^aRE denotes relay.^bPB denotes push button.

Detailed diagrams of the fault tree analyzed in this study are given in Appendix B.

The primary objective of this analysis is to show that the reactor can experience the prescribed startup accident and still withstand one additional failure. The conditions for the prescribed startup accident are set forth in Sec. 15.2.2 of the LPTR Safety Analysis Report¹ as follows:

1. The reactor is initially shut down.
2. The shim rods are withdrawn simultaneously at their maximum rate.

3. All period and high level scrams and rundowns fail except the level-safety fast scram at 150% of full power.

4. The shim rods continue out for 20 msec (the measured delay time) after the 150% power level has been reached and then fall into the core with an acceleration of 5.2 m/s^2 .

Simulation of the startup accident as defined above is readily accomplished in either of two ways:

1. All houses representing power ≥ 4.5 MW are turned on (tau set equal to 1), and all houses representing period

Table 2. Rates input conditions for computer runs.

HOUSES & HOUSEHOLDS	
H-102	110441 BULLY
H-108	110441 BULLY
H-101	110441 BULLY
H-105	110441 BULLY
H-106	110441 BULLY
H-107	110441 BULLY
H-108	110441 BULLY
H-109	110441 BULLY
H-110	110441 BULLY
H-111	110441 BULLY
H-112	110441 BULLY
H-113	110441 BULLY
H-114	110441 BULLY
H-115	110441 BULLY
H-116	110441 BULLY
H-117	110441 BULLY
H-118	110441 BULLY
H-119	110441 BULLY
H-120	110441 BULLY
H-121	110441 BULLY
H-122	110441 BULLY
H-123	110441 BULLY
H-124	110441 BULLY
H-125	110441 BULLY
H-126	110441 BULLY
H-127	110441 BULLY
H-128	110441 BULLY
H-129	110441 BULLY
H-130	110441 BULLY
H-131	110441 BULLY
H-132	110441 BULLY
H-133	110441 BULLY
H-134	110441 BULLY
H-135	110441 BULLY
H-136	110441 BULLY
H-137	110441 BULLY
H-138	110441 BULLY
H-139	110441 BULLY
H-140	110441 BULLY
H-141	110441 BULLY
H-142	110441 BULLY
H-143	110441 BULLY
H-144	110441 BULLY
H-145	110441 BULLY
H-146	110441 BULLY
H-147	110441 BULLY
H-148	110441 BULLY
H-149	110441 BULLY
H-150	110441 BULLY
H-151	110441 BULLY
H-152	110441 BULLY
H-153	110441 BULLY
H-154	110441 BULLY
H-155	110441 BULLY
H-156	110441 BULLY
H-157	110441 BULLY
H-158	110441 BULLY
H-159	110441 BULLY
H-160	110441 BULLY
H-161	110441 BULLY
H-162	110441 BULLY
H-163	110441 BULLY
H-164	110441 BULLY
H-165	110441 BULLY
H-166	110441 BULLY
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H-170	110441 BULLY
H-171	110441 BULLY
H-172	110441 BULLY
H-173	110441 BULLY
H-174	110441 BULLY
H-175	110441 BULLY
H-176	110441 BULLY
H-177	110441 BULLY
H-178	110441 BULLY
H-179	110441 BULLY
H-180	110441 BULLY
H-181	110441 BULLY
H-182	110441 BULLY
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H-187	110441 BULLY
H-188	110441 BULLY
H-189	110441 BULLY
H-190	110441 BULLY
H-191	110441 BULLY
H-192	110441 BULLY
H-193	110441 BULLY
H-194	110441 BULLY
H-195	110441 BULLY
H-196	110441 BULLY
H-197	110441 BULLY
H-198	110441 BULLY
H-199	110441 BULLY
H-200	110441 BULLY

≤5 sec are also turned on. Diamond D-200 and component C9LNIONC, which represents the log N compensated ion chamber, are turned on. This effectively falls all period and slow scrams (run-downs are not included in the fault tree analysis of the scram system), leaving only the 4.5-MW fast scram (150% of full power) to scram the reactor (see computer run 16, Appendix C).

2. A second method is to enable only one scram condition, i.e., house 702 representing power ≥4.5 MW. (House 704, the complement of house 702, is also turned off.) This effectively bypasses all scrams except the level-

safety fast scram at 150% of full power (computer run 15, Appendix C).

Both computer runs were made and the results for both were identical, as predicted.

For the startup accident prescribed in Sec. 15.2.2 of the LPTR Safety Analysis Report,¹ there are two single events, either of which will result in the top event, i.e., cause two or more shim rods to fail to fully enter the core; these are diamonds D-100 and D-702. Each of these events is considered to be outside the limits of credible events. (See diamond notes 2 and 8, in Appendix B.)

Conclusion

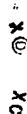
There are no single component failures which can result in failure of the reactor to scram for the prescribed startup accident. There are also no pairs of components which can result in failure to scram.

As a minimum, failure of three independent components — one in each of the three level-safety fast scram channels — would be required to produce a scram failure that could result in release of fission products within the reactor containment dome.

Appendix A. Control System Diagrams for the LPTR

Reproduced here are pages 8, 13, 14, and 24 of the LEA-01-3154-01 series of drawings of the LPTR control system:

Automatic Rundown and Scram Circuits (p. 8)	10
Amplifier Trouble Monitor and Experiment Scram Alarm Circuits (p. 13)	11
Monitor Alarm and Scram Circuits (p. 14)	12
Safety Amplifiers and Safety Interlock Chain (p. 24)	13



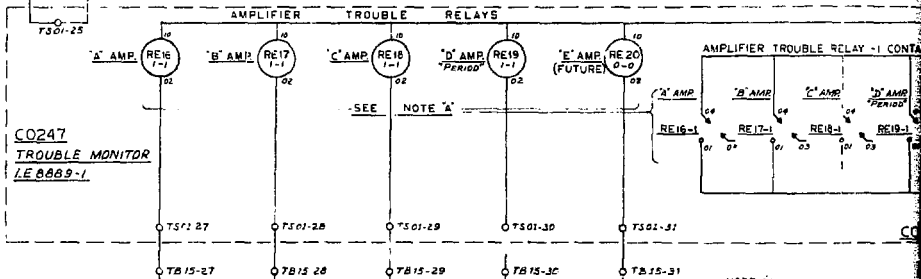
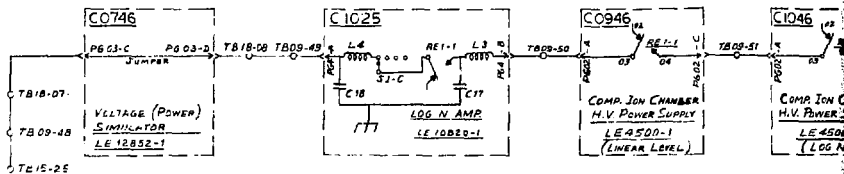
-10-

AMPLIFIER TROUBLE MONITORING

22VAC

LC

22VDC
FROM P11



C0247
TROUBLE MONITOR
LE 8889-1

NOTE A:

	CONTACTS SHOWN ON PANEL		
	-1	-2	-3
RE 16	13	24	NOT USED
RE 17	13	24	"
RE 18	13	24	"
RE 19	13	24	"
RE 20	NOT USED	NOT USED	"

SEE NOTE B, PAGE 17, FOR CONNECTION DIAGRAM OF C0247 RELAYS RE 16 THRU 20.

NOTE B:

IN AMPLIFIER A, B, C, D, AND E, CONTACT J6 IS INSULATED FROM THE CHASSIS. FINAL PATCH SIGNAL BUS MUST BE CONNECTED. C0247 RELAYS 16 THRU 20 CAN BE

PAGE
13

RG-59/U PATCH
CABLES WITH
BNC CONNECT-
TERS & PLUGS

GROUND
SEE R10

L12

L11

SIGMA BUS CONDUIT & OUTLET BOXES - REAR OF CONSOLE

DEMULTIPLEXER
SEE
LE 4552-1

TO C0230,
PG 12-100
DROP TESTER
LE 10332-1

ANG-1

TO C0246,
PG 12-100
DROP TESTER
LE 10332-1

NOTE C:

TS1-30
IN WIRE
SHUTTLE
SWITCH
CIRCUIT
RE 17
SEE

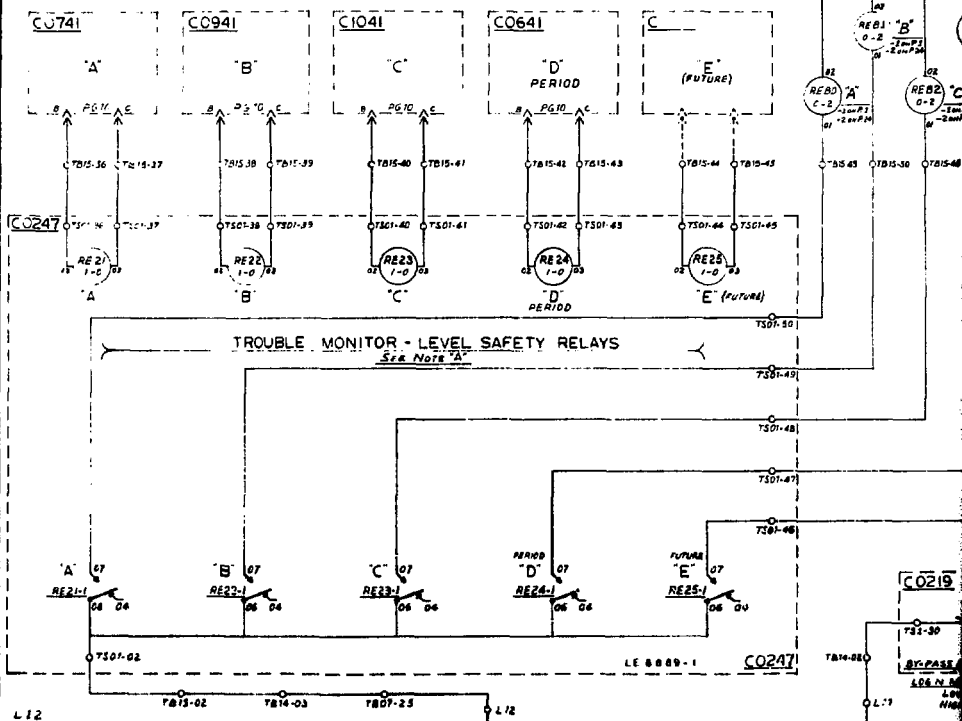
LE 401354-01-E
PAGE 13

Fig. A-2. Amplifier trouble monitor and experiment alarm circuit (p. 13).

LEVEL & PERIOD SAFETY AMPLIFIERS

LEVEL SAFETY SCRAM

SAFETY AMPLIFIERS - LE 5624-1



L 12

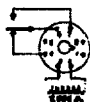
PAGE
14

L 11

NOTE: IN
COAST-PROBLEM
MONITORING-LE 5624-1
RE 21 TROUBLE RE 23
LE 5624-1

L 207

LE 5624-1
PLATE RELAY



LE 5624-1
PLATE RELAY

LE 5624-1
PAGE 14

- LOG N, LINEAR LEVEL, & POOL WATER LEVEL

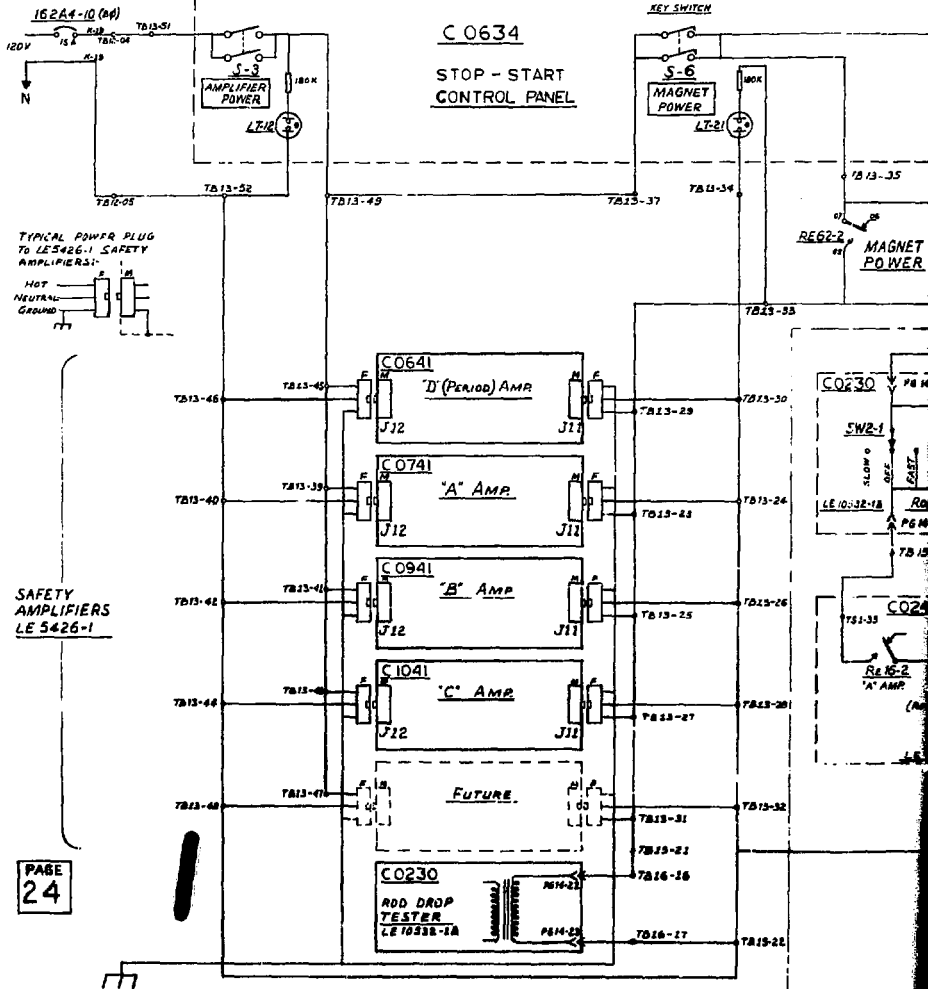


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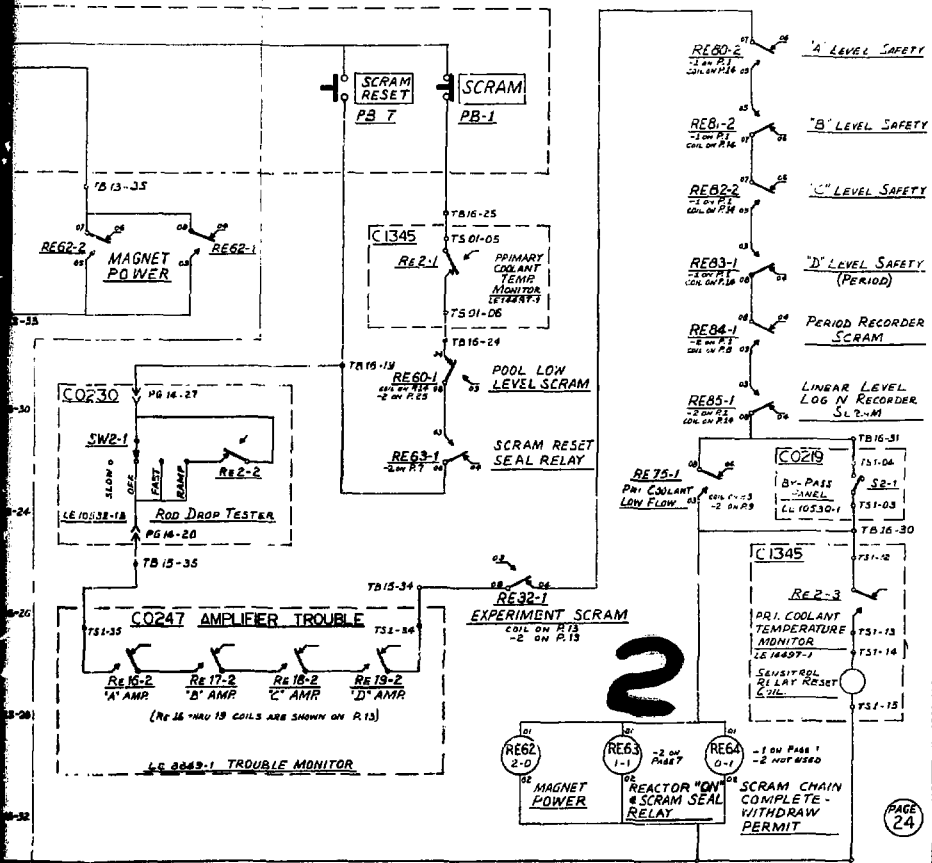
LEA	DI-3154	Q1	SF
100	400 015401-XF	INSET 14 of 25	

- 12 -

SAFETY AMPLIFIERS



SAFETY INTERLOCK CHAIN



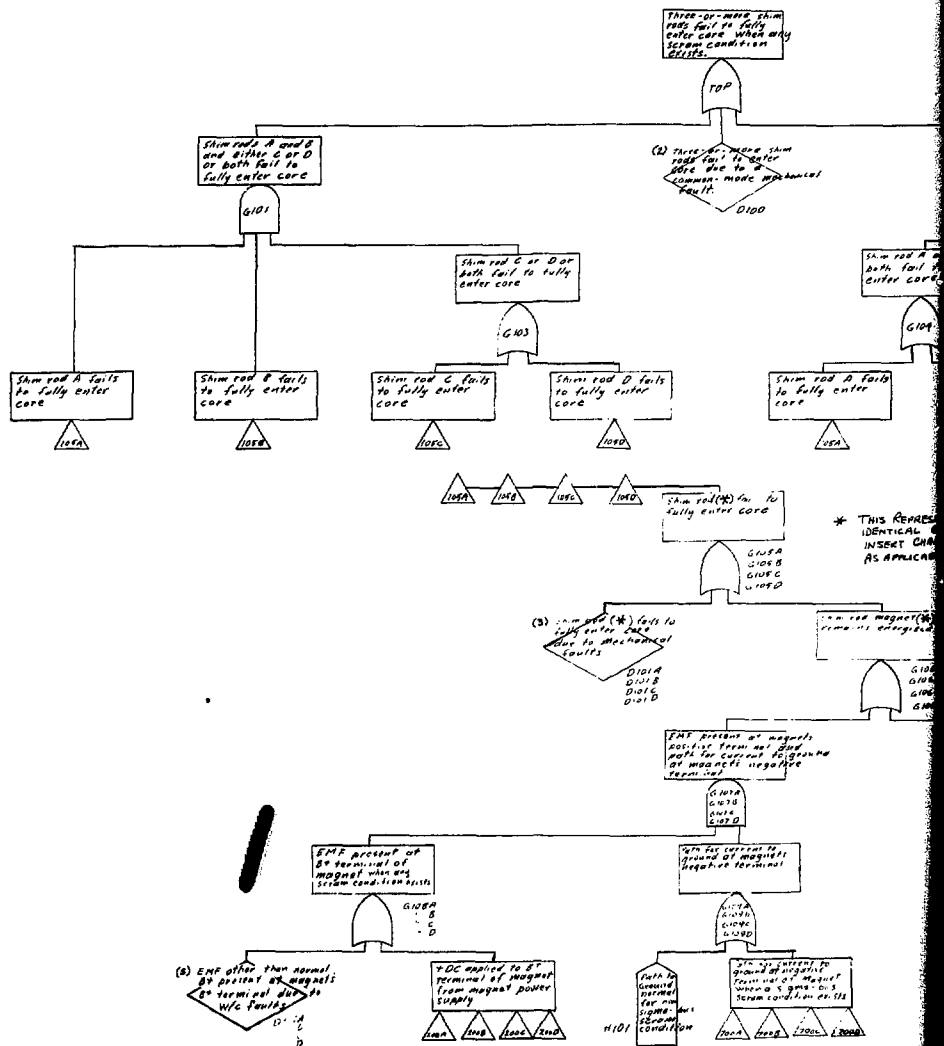
PAGE 24

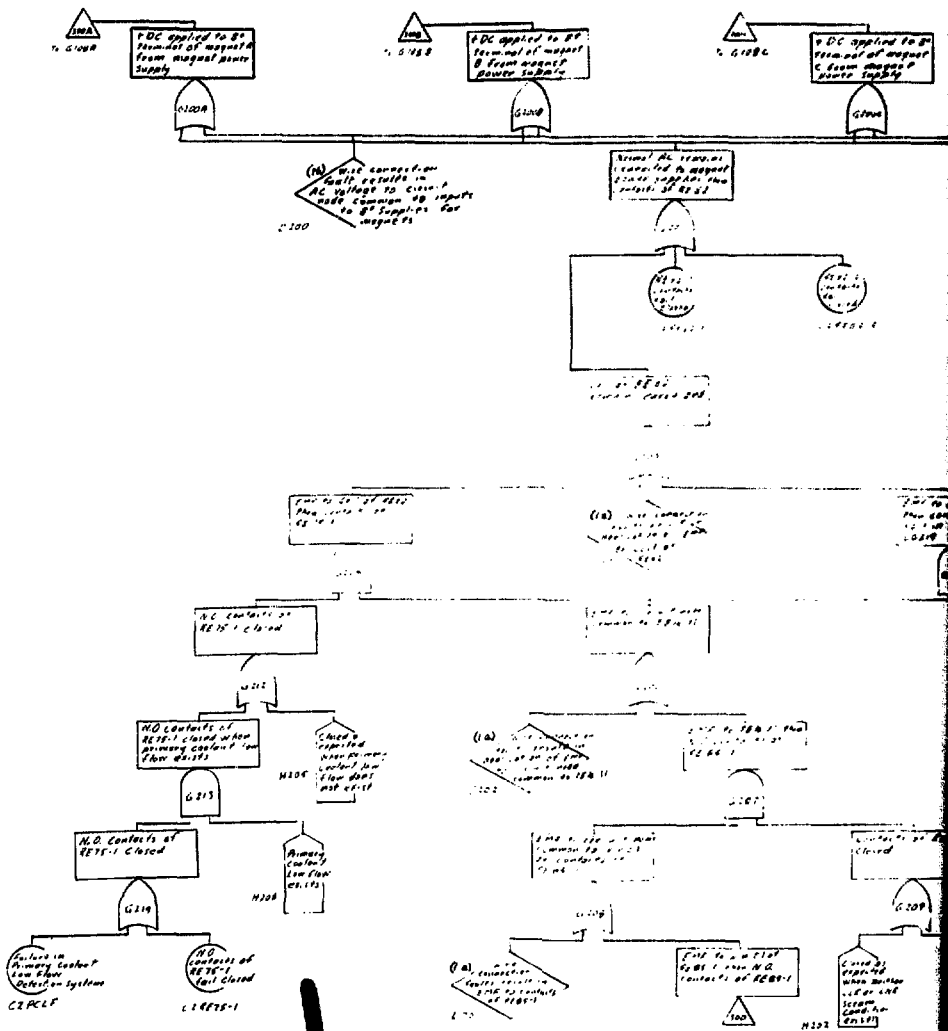
DRAWN BY RCG CHECKED BY J. RYU DATE 9-78 APPROVED BY J. RYU DATE 4-74	ALL CORRECTED & REDRAWN SAFETY AMPLIFIERS & SAFETY INTERLOCK CHAIN UNIVERSITY OF CALIFORNIA LAWRENCE RADIATION LABORATORY ELECTRONIC ENGINEERING DEPARTMENT LIVERMORE, CALIFORNIA 94550	DATE 9-78 DRAWN J. RYU CHECKED J. RYU DATE 4-74 APPROVED J. RYU DATE 4-74	GROUP NAME LEA01-3154-01-SF GROUP NO. 1 REV. 1 DATE 9-78 BY J. RYU CHECKED J. RYU DATE 4-74
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Fig. A-4. Safety amplifiers and safety interlock chain (p. 24).

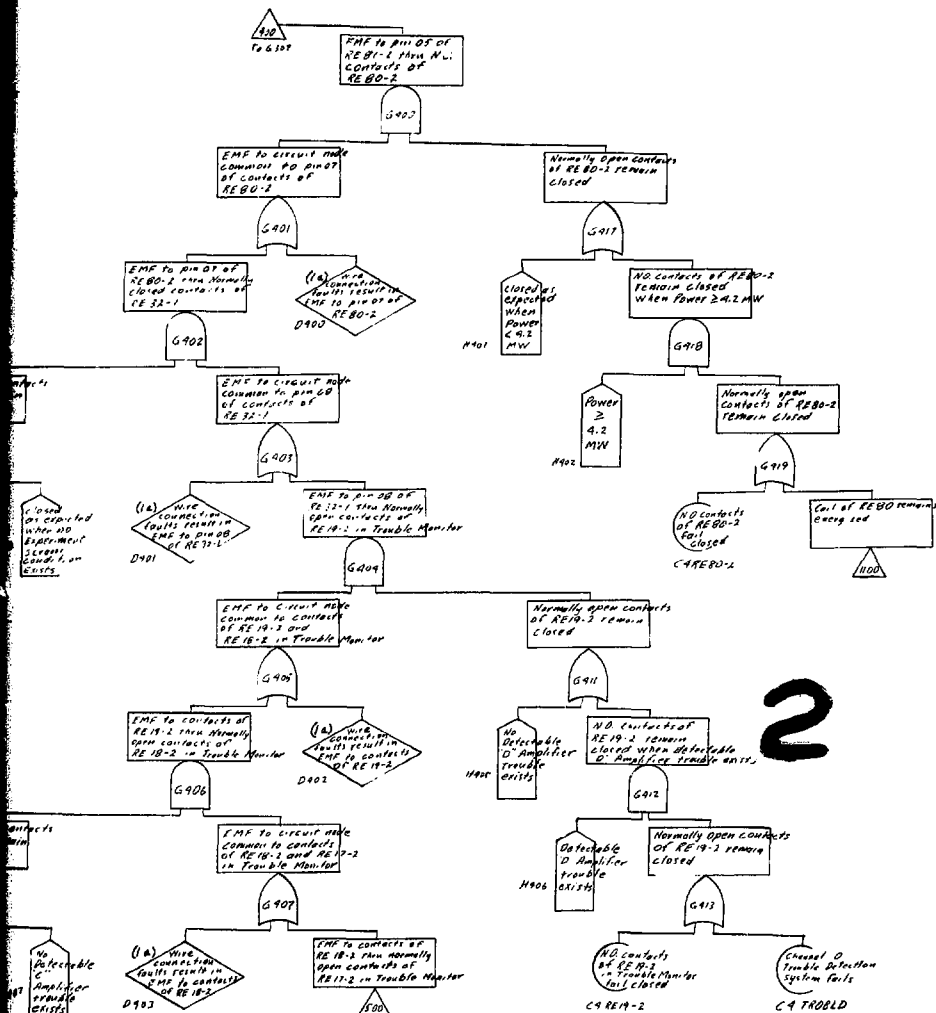
Appendix B. Fault Tree Analyzed in This Study

The fault tree analyzed in this study is diagrammed on the following 11 pages, labeled sheets 1 through 11. Numbers in parenthesis by the diamonds refer to "diamond notes" which are listed beginning on p. 26.

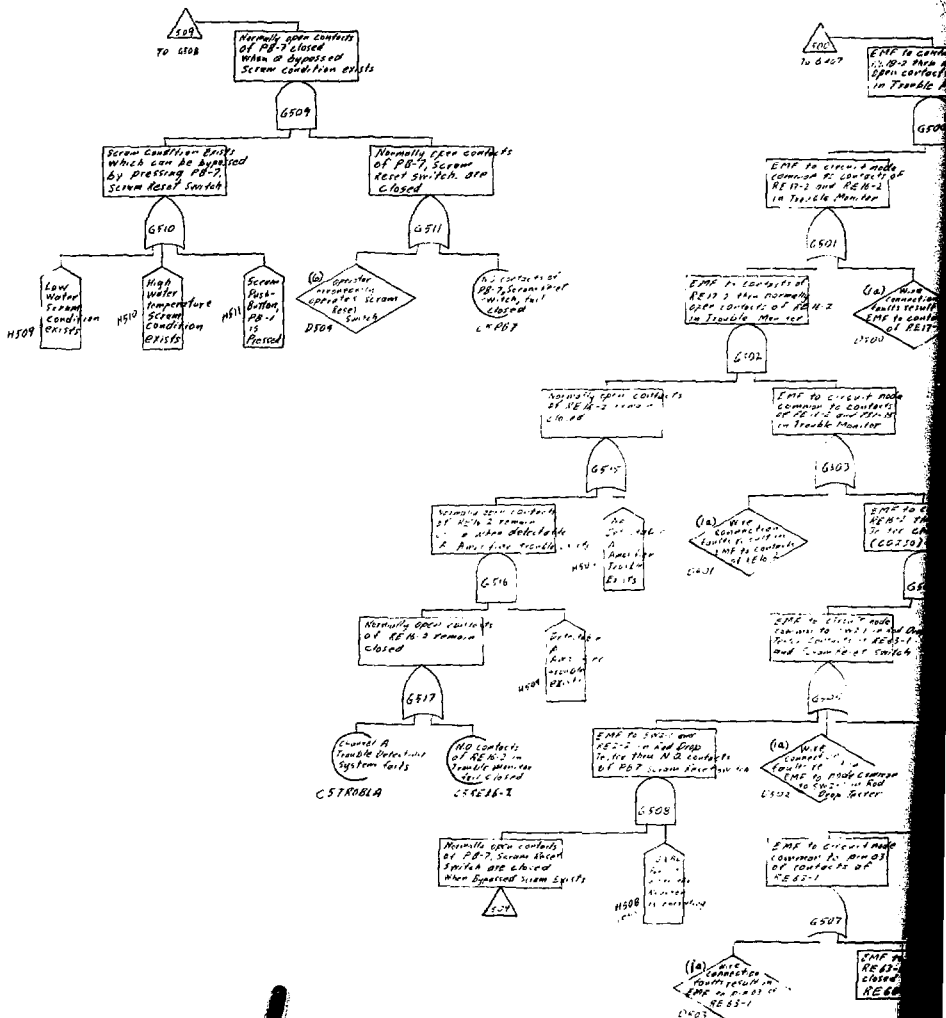






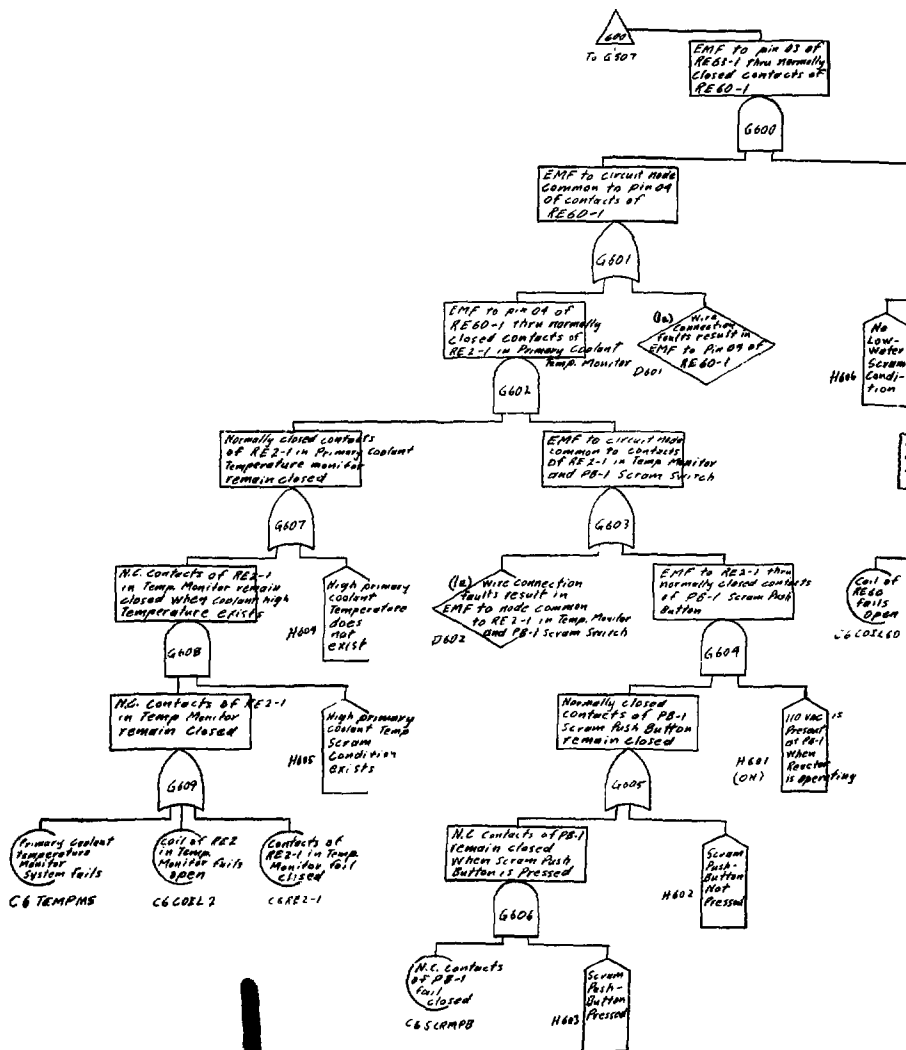


Fault tree for LPTR scram system (sheet 4).





- 19 -



Fault tree for LPTR scram system

700A 700B 700C 700D
1. G110A 1. G110B 1. G110C 1. G110D

See for control to
ground "1" input of
transistor of Magnet
A in Sigma Bus
Control Logic

G110A
G110B
G110C
G110D

(7) When connection
faults occur in
Sigma Bus for control
of Magnet
G110A
G110B
G110C
G110D

Magnet Amplifier
controls when there
is a fault in Sigma Bus
control logic

Magnet Amplifier
controls when there
is a fault in Sigma Bus
control logic

Magnet Amplifier
controls when there
is a fault in Sigma Bus
control logic

Time
5 Sec
N701

Magnet Amplifier
controls

Time
5 Sec
N702

Time
5 Sec

No Sigma Bus input to
Sigma Amplifier A

(8) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier A

No Sigma Bus input to
Sigma Amplifier A

No Sigma Bus input to
Sigma Amplifier A
N705
(out)

Sigma Amplifier A
does not apply a
Sigma Bus input to
Sigma Amplifier A

Sigma Amplifier B
does not apply a
Sigma Bus input to
Sigma Amplifier B

(9) Sigma Bus A
fails in special
manner which does not
cause trouble
N706
Time for Sigma

No Sigma Bus input to
Sigma Amplifier A

(10A) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier A
D707
Time for Sigma

(10B) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier B
D708
Time for Sigma

(10C) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier C
D709
Time for Sigma

(10D) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier D
D710
Time for Sigma

(10A) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier A
D707
Time for Sigma

No Sigma Bus input to
Sigma Amplifier A

(10B) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier B
D708
Time for Sigma

(10C) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier C
D709
Time for Sigma

(10D) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier D
D710
Time for Sigma

(10E) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier E
D711
Time for Sigma

(10A) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier A
D707
Time for Sigma

No Sigma Bus input to
Sigma Amplifier A

(10B) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier B
D708
Time for Sigma

(10C) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier C
D709
Time for Sigma

(10D) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier D
D710
Time for Sigma

(10E) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier E
D711
Time for Sigma

(10A) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier A
D707
Time for Sigma

No Sigma Bus input to
Sigma Amplifier A

(10B) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier B
D708
Time for Sigma

(10C) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier C
D709
Time for Sigma

(10D) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier D
D710
Time for Sigma

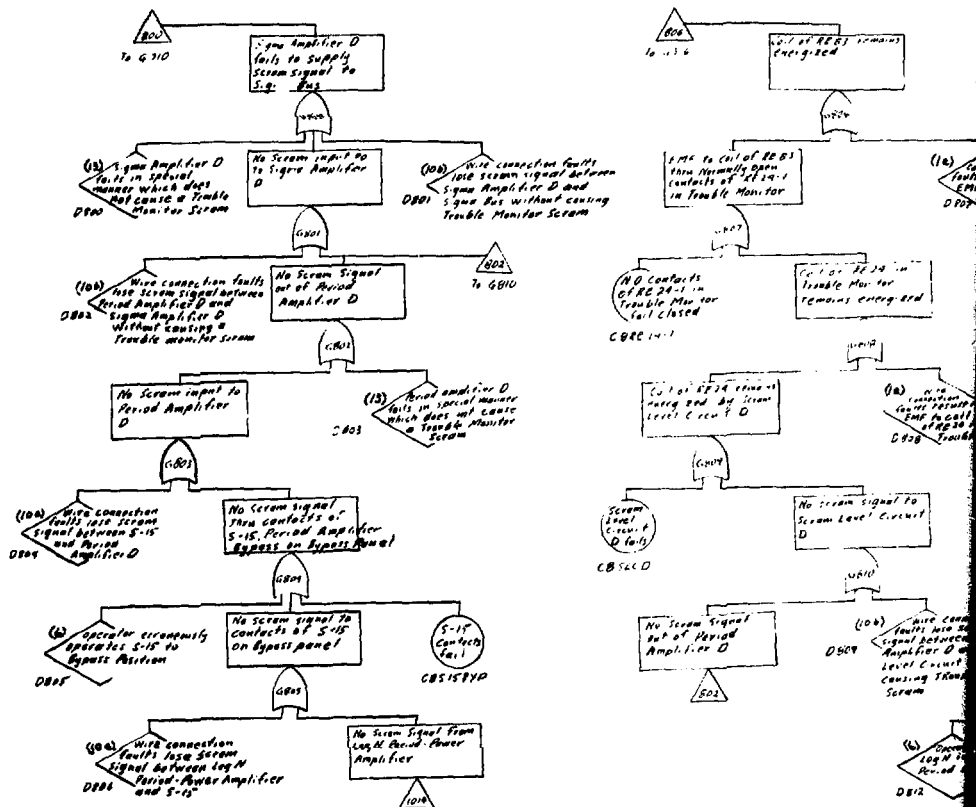
(10E) No connection
faults occur in Sigma Bus
for Sigma Bus input to
Sigma Amplifier E
D711
Time for Sigma

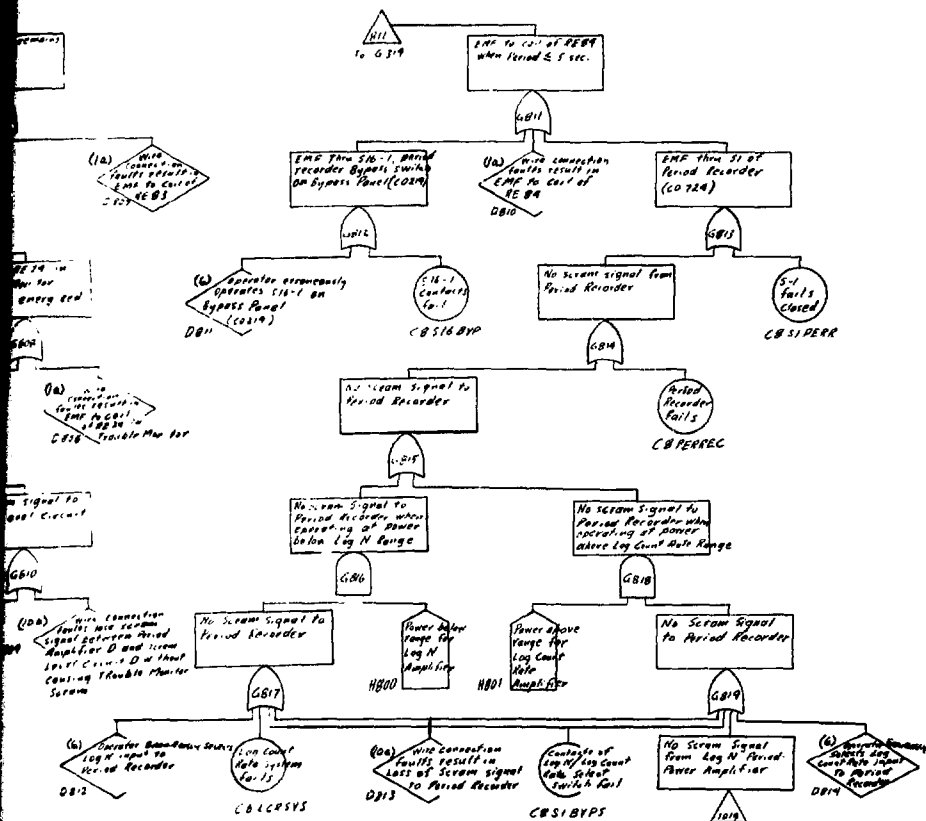
System A
fails
N707
Time for Sigma

System B
fails
N708
Time for Sigma

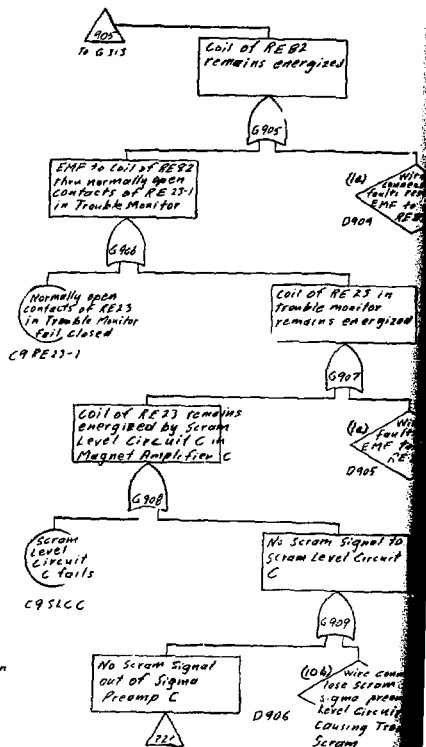
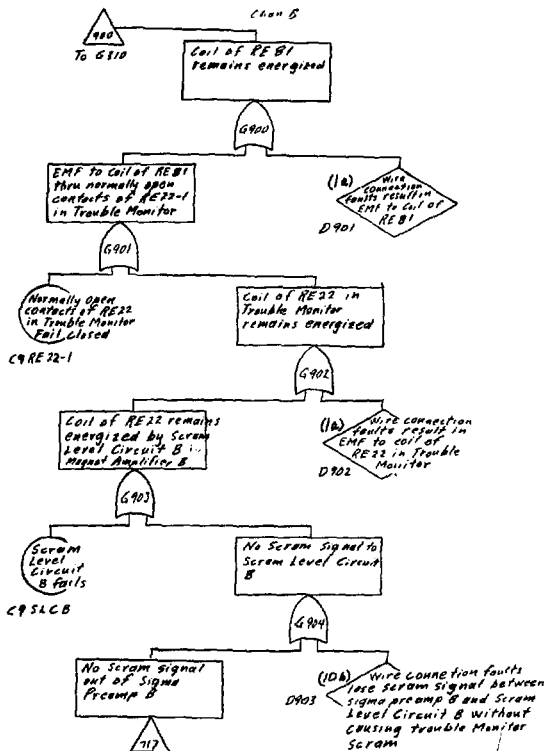
System C
fails
N709
Time for Sigma

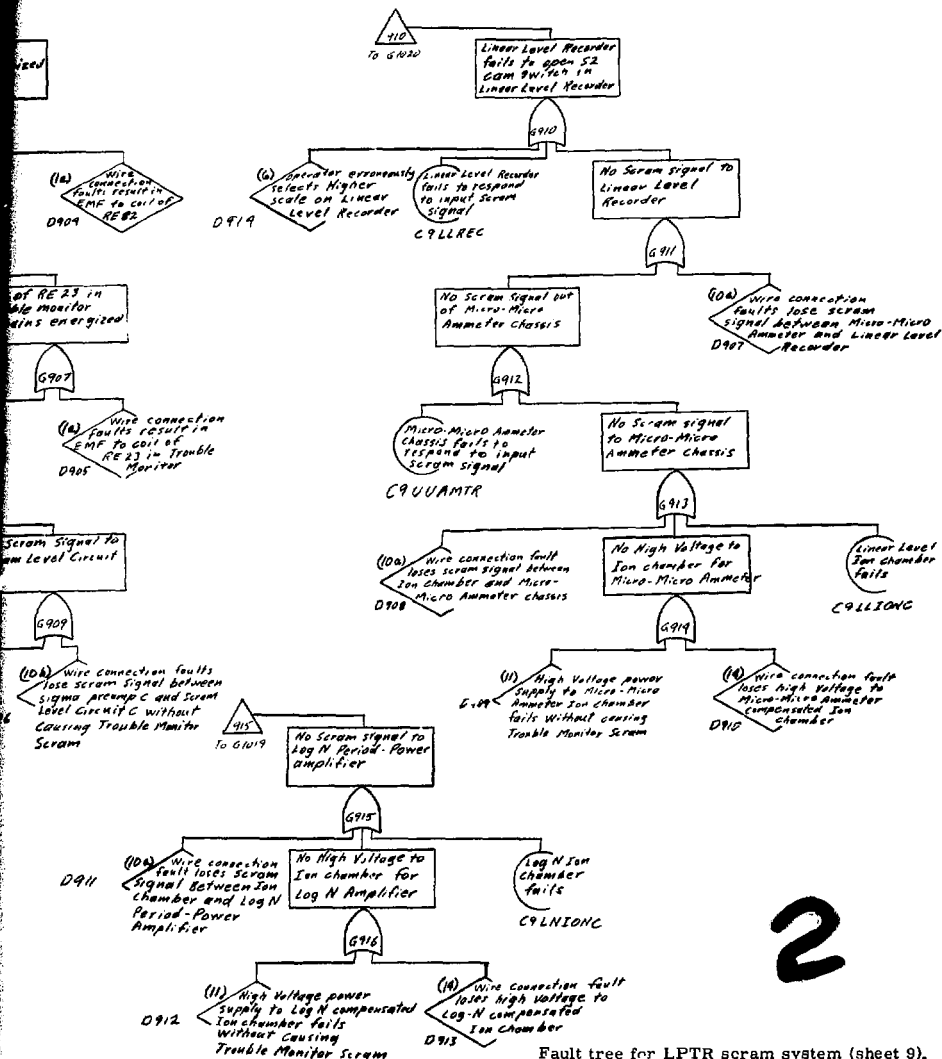
System D
fails
N710
Time for Sigma



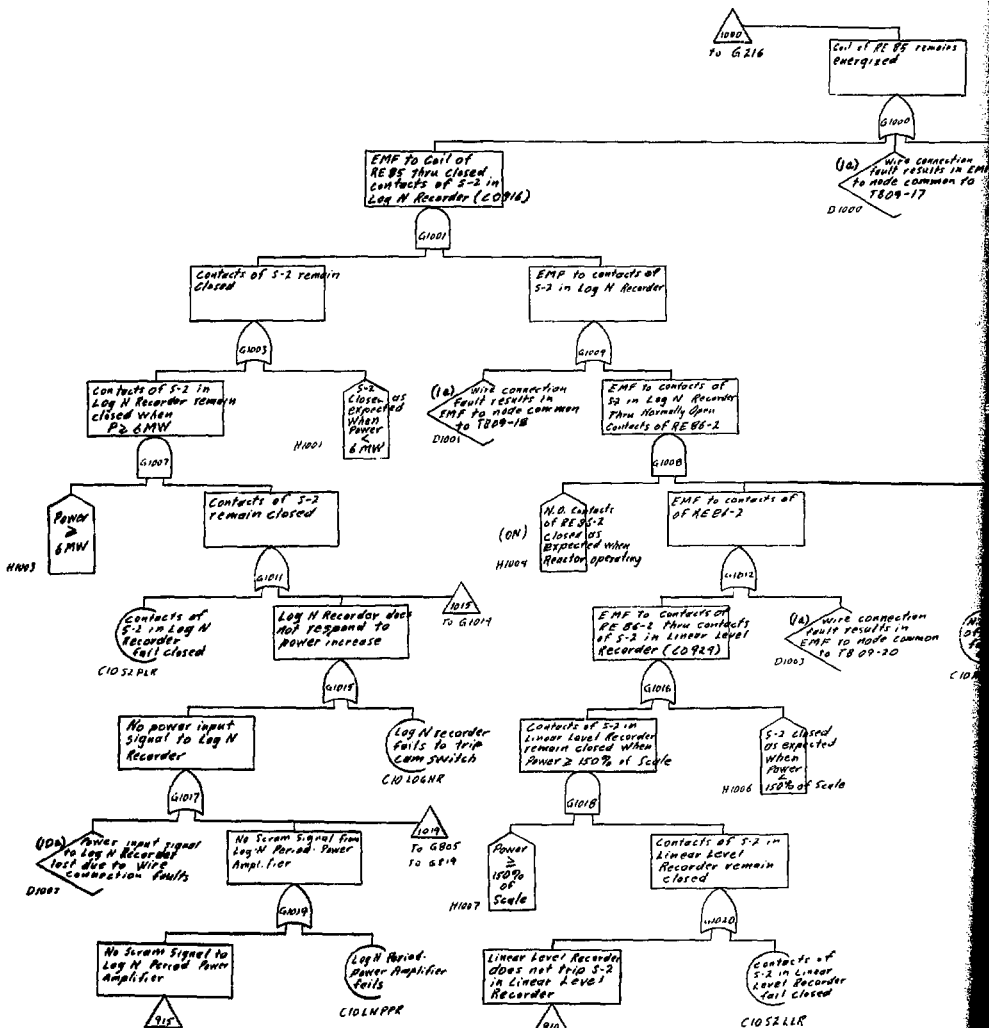


Fault tree for LPTR scram system (sheet 8).



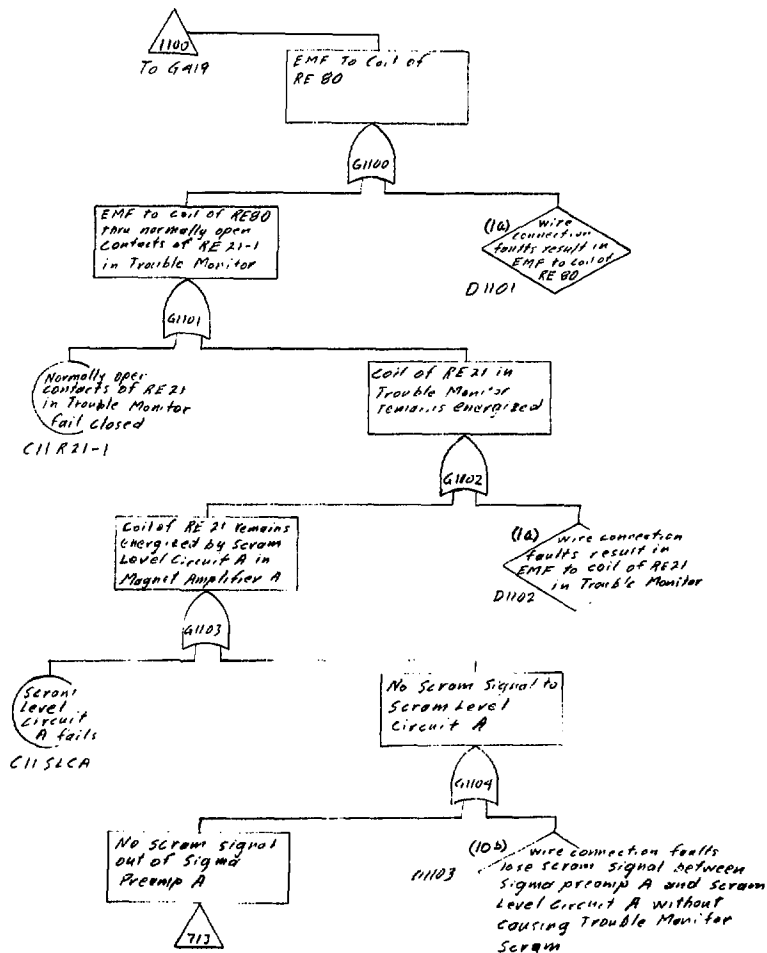


Fault tree for LPTR scram system (sheet 9),





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Fault tree for LPTR scram system (sheet 11).

DIAMOND NOTES

1. a. A wiring or connection fault is assumed which places an unwanted emf at a particular point in the circuit as described in the diamond. The undesired emf causes a circuit response which prevents a scram operation from occurring. The emf can be ac or dc at any level sufficient to produce the undesired result.

b. In this case, the undesired emf must be ac applied at any point to the node common to terminal 1 of transformer T-2 in any one of the four safety amplifiers, all the way to pins 03 and 05 of relay 62. Such a fault energizes all four magnet power supplies and prevents the shim rods from dropping via the slow scram system.

2. This diamond (D-100) was included for two reasons. The first reason is to provide a test for those computer runs in which without D-100 there would have been no minimal cut sets. (A cut set is a collection of one or more events which will cause the top event to occur.) Every computer run will have at least one cut set involving a single failure (D-100), thus providing a degree of assurance that the computer run was properly executed. The second reason for including D-100 is to give consideration to any common mode failure which might result in three or more shim rods failing to enter the core after all four had been released from the supporting magnets. The event represented by D-100 is considered to be an incredible event. It seems unlikely that even an earthquake could deform or tilt the core sufficiently to cause the rods to bind and fail to insert fully. Core melt is not a credible mechanism, as is shown by the analyses in chapter 15.2.1 in Ref. 1.

3. This fault can be caused by any mechanical failure or obstruction which would prevent an individual shim rod from dropping into the core.

4. This fault requires that an extremely unlikely combination of wire connection faults occur simultaneously so as to place an emf at the V7 and V8 terminals of the magnets and a current sink at the B⁺ terminals, which is the opposite of the normal connections. It is included for completeness, but is considered to be incredible.

5. The magnets will hold the shim rods in place with either ac or dc current flowing (dc is normal). This fault requires a wire connection fault that places at the magnet B⁺ terminals an ac or dc emf that provides sufficient current to energize the magnet and not burn it open.

6. This fault is caused by an operator deliberately but erroneously actuating the device described in the diamond. This either places the circuits in a state which prevents them from responding as they should to cause a scram, or else alters or bypasses the equipment or circuitry in a manner which prevents a scram.

7. Shim rod drop is normally caused by cutting off the magnet current at a point downstream from the negative terminal. The fault described in this diamond provides an unwanted alternate return path which bypasses the normal switching circuit and therefore allows magnet current to flow during a scram condition when it is not supposed to flow.

8. This fault represents a wiring connection fault that results in the shorting of the sigma bus to a low impedance source of emf in the range between +22 and +45 V dc. No such low-impedance source of emf within this range exists in the vicinity of the sigma bus or the sigma amplifiers. (A short to ground or dc voltage greater than +45 V results in a scram.) An open circuit between the sigma bus and magnet amplifier results in the cutoff of that magnet amplifier. A short to a voltage divider resulting in the required +22 to +45 V would be driven out of range by the cathode-follower output of the sigma amplifiers. The event represented by diamond 702 is considered to be incredible, but is included for completeness.

9. This failure would require coincident events to occur along with the power supply failure since the proper power-supply voltage level is monitored by a trouble monitor relay. This event might be a wiring connection fault or a relay fault. It is credible but unlikely.

10. a. Loss of signal or voltage can be caused by open- or short-circuit wiring connection faults which prevent the equipment being fed from detecting that a scram condition exists.

b. If such a loss of scram signal would normally initiate a trouble-monitor slow scram, the coincident wiring connection or relay faults must also exist which would prevent the trouble monitor scram from occurring. This is credible but unlikely.

11. A failure of the HV supply to the ion chambers prevents them from detecting a scram condition, and the power supply low-voltage monitor normally initiates a slow scram. This fault, therefore, requires a coincident wire connection or relay failure in the monitoring circuit, such that the expected trouble-monitor scram does not occur. This is considered credible but unlikely.

12. This fault is a wire connection open- or short-circuit fault which prevents the normal emf required for circuit operation from reaching the relay coil.

13. The composite safety amplifiers are normally monitored for proper operation by relays in the composite amplifier or by the input signal getting out of normal operating range, either of which would trip the slow scram or trouble-monitor scram circuits. This failure, therefore, requires the coincident failure of the trouble-monitor circuits by wiring-connection or relay faults which prevent trouble-monitor scram from occurring. This is credible but unlikely.

14. Any wire connection short or open circuit in the ion chamber's HV power supply leads will inhibit ion chamber operation, and so prevent it from transmitting a scram level signal.

Appendix C. Results of Computer Analysis of Fault Tree

Table C-1 lists the 17 computer runs made on the fault tree considered in this study and summarizes the results of each run. Computer printouts of the cut sets for the 17 runs are reproduced at the end of this appendix.

Table C-1. Summary of the computer runs made in the fault tree analysis of the LPTR scram system. The top event is defined as three or more shim rods failing to fully enter the core when a scram condition exists.

Computer run	Assumption	Number of single faults producing top event	Number of double faults producing top event
1	Power <4.5 MW, period 1 sec (tests -sigma bus scram functions and power and slow scrams)	1 (D-100)	5
2	Same as run 1, except that log X channel is assumed failed or bypassed initially	1 (D-100)	5
3	Power >6 MW	1 (D-100)	5
4	Power >4.5 MW, reached gradually	1 (D-100)	8
5	Fast period (<1 sec) during startup, while in low power range (<10 kW)	1 (D-100)	184
6	Same as run 5 except for higher power range (>100 kW)	6 (D-100, -912, -911, -913, C9LN10NC, C10LNPPR)	99
7	Low-primary-coolant-flow scram condition	9	None
8	Experiment scram condition	15	None
9	Low-primary-coolant-level scram condition	24	None
10	High-primary-coolant-temperature scram condition	25	None
11	Actuation of manual scram push button	24	None
12	Power exceeds three-fourths of full scale (linear)	27	None
13	Same as run 12, plus fast period (<1 sec)	1 (D-100)	None
14	Same as run 13 except reactor in high power range	1 (D-100)	None
15	Failure of slow scram and fast period scram, resulting from failure to turn on these scram gates	2 (D-100, -702)	None
16	Same as run 15, but resulting from failed components	2 (D-100, -702)	None
17	Same as run 15, but testing for triple failures	2 (D-100, -702)	None (716 triples)

The computer runs of greatest significance to this study are runs 15, 16, and 17. Run 16 represents the specified startup accident. Initial conditions for the computer data deck (see Table 2) represent the failure of the slow scram chain (D-200) and the fast period channel (log N ion chamber failed). Under these conditions, the reactor is scrammed by any one of the three power-level channels through the sigma bus and magnet amplifiers. The computer run results in two single failures which can cause a failure to scram. These are represented by diamonds D-100 and D-702. The diamond notes 2 and 8 (Appendix B) explain why these events are unlikely.

Computer run 15 also simulates the specified startup accident by a different method, but with results identical to run 16. Instead of failing components in the fault tree as was done in run 16, in run 15 the gates which enable the slow scram chain and the fast period scram are not turned on. This simulates failure of the slow scram mechanism (in which B^+ voltage is removed from the magnet coils) and the fast-period scram channel.

Computer run 17 uses the same rates (failure data) input as used in run 15, but tests for combinations of triple failures. The run reveals a total of 716 combinations of triple failures which will result in failure to scram for the specified startup accident. (The specified startup accident postulates failure of the slow scram chain and fast period channel as initial conditions. These are in addition to the triple component failures.) The 716 combinations of triple failures consist of combinations, taken three at a time, of elements represented by circles and diamonds in the three redundant power-level scram channels A, B, and C. The bulky tabulation of these cut sets is not included in the report.

Computer run 1 and runs 3 through 14 represent normal scram conditions with no assumed initial failure.

Computer run 1 represents both high power (≥ 4.5 MW) and fast period (≤ 1 sec). This is a test of the sigma bus scram functions. In addition, the period and power slow scrams also are tested (power ≥ 4.2 MW and period ≤ 1.2 sec), since these conditions are included in the assumed initial conditions. For this scram condition, there are no credible single or double failures. The incredible failures which result from this run include D-100 as the only single, and D-702 in conjunction with a failure of the slow scram chain.

Computer run 2 is the same as run 1 except that the log N channel is assumed failed or bypassed initially. The results for run 2 are identical with the results for run 1. This shows that the reactor can operate safely and withstand a single failure even with the period scram channel bypassed or failed.

Computer run 3 assumes the power has exceeded the 200% (6-MW) level. This introduces one additional slow scram. This scram mechanism does not affect the failure analysis as far as single and double failures are concerned. The results are identical with those of computer runs 1 and 2.

Computer run 4 assumes the power has exceeded the 150% (4.5-MW) level gradually without generating a 20-sec-period rundown or a 1-sec-period scram. The cut sets for this run include all those for run 1, plus three additional double failures

Involving diamond 702 in conjunction with components in the slow scram chain. The interpretation of this result is essentially the same as that for computer run 1, i.e., there are no credible single or double failures which will result in a failure to scram.

Computer run 5 assumes a fast period (≤ 1 sec) during startup, while in the low power range (≤ 10 kW), i.e., before switching from the log-count-rate period amplifier to the log-N period amplifier. The run tests the ability of the system to withstand single and double failures and scram the reactor before power reaches the 150% level. (Run 1 covers the case of fast period on startup where power exceeds 150%.) There are no credible single failures which can result in failure to scram. There are 184 combinations of double failures (including six involving the incredible event represented by D-702) which could result in failure to scram before reactor power reaches the 150% level.

Computer run 6 assumes the same condition as run 5 except that the analysis is for the power range after the operator has switched from the log-count-rate period amplifier to the log-N period amplifier (power > 100 kW). This run results in single failures in the log-N period/power amplifier channel which could result in failure to scram before power reaches the 150% level. Any single component in this channel which results in failure of the channel to function results in a failure to scram under these conditions. In run 15 this channel is assumed failed for the specified startup accident.

Computer runs 7 through 12 each test a scram function on the slow scram chain. These conditions are not sensed on the fast scram (sigma bus) circuitry. Therefore, in each case there are several single failures that result in failure of a particular scram condition to bring about a scram. These include failure of the contacts of relay 62 (RE-62) to open, shorts to ac voltage in the magnet power supply circuitry, shorts to ac power on the relay scram chain, and failure of the contacts of the relay for that particular scram function to open. In each case only a single failure is required as this is a single, series relay chain.

Computer run 7 assumes the low-primary-coolant-flow scram condition. This run results in nine cut sets representing single failures.

Computer run 8 assumes the experiment scram condition. This run results in 15 cut sets representing single failures.

Computer run 9 assumes the low-primary-coolant-level scram condition and results in 24 cut sets representing single failures.

Computer run 10 assumes the high-primary-coolant-temperature scram condition. This run results in 25 cut sets representing single failures.

Computer run 11 assumes the actuation of the manual scram push button. This run results in 24 cut sets representing single failures. There are several ways the operator can scram the reactor if the scram system should fail to respond to the manual scram push button. These are discussed in the operator's procedures for the LPTR.

Computer run 12 assumes that the power level exceeds the level represented by three-fourths of full scale on the linear level recorder. This function is sensed on the slow scram chain only. This run results in 27 cut sets representing single failures.

Computer run 13 assumes the same condition as in run 12, plus the assumption of a fast period (≤ 1 sec). The reactor power is in the low power range, i. e., the period recorder is still connected to the log-count-rate meter. This run results in no credible single or double failures which can prevent reactor scram. The diamond D-100 is in the only cut set found.

Computer run 14 is the same as run 13 except that the reactor is in the high power range, i. e., the period recorder has been switched to the log N channel. The results of this run are identical with those of run 13.

The cut sets for the 17 computer runs are reproduced on the following pages.

COMPUTER PRINTOUTS LISTING CUT SETS AND COMPONENTS FOUND IN CRITICAL PATHS

Runs 1, 2, 3

```

1
*****
MINIMAL CUT SETS FOUND BY COMBO FOR LPTA FAULT TREE SAFETY ANALYSIS
*****
CUT SET * 1 D100
CUT SET * 2 D202 D702
CUT SET * 3 D201 D702
CUT SET * 4 C2RE62-1 D702
CUT SET * 5 C2RE62-2 D702
CUT SET * 6 D200 D702
*****
END OF CRITICAL PATHS *****

```

```

1
*****
CRITICAL COMPS FOUND IN PATHS
*****

```

D702 D202 D201 C2RE62-1 C2RE62-2 D200 D100

Run 4

```

1
*****
MINIMAL CUT SETS FOUND BY COMBO FOR LPTA FAULT TREE SAFETY ANALYSIS
*****
CUT SET * 1 D100
CUT SET * 2 D301 D702
CUT SET * 3 D300 D702
CUT SET * 4 D203 D702
CUT SET * 5 D202 D702
CUT SET * 6 D201 D702
CUT SET * 7 C2RE62-1 D702
CUT SET * 8 C2RE62-2 D702
CUT SET * 9 D200 D702
*****
END OF CRITICAL PATHS *****

```

```

1
*****
CRITICAL COMPS FOUND IN PATHS
*****

```

D702 D301 D300 D203 D202 D201 C2RE62-1 C2RE62-2 D200 D100

Run 5

```

1
*****
MINIMAL CUT SETS FOUND BY COMBO FOR LPTA FAULT TREE SAFETY ANALYSIS
*****
CUT SET * 1 D100
CUT SET * 2 C8LCRSYS D912
CUT SET * 3 C8LCRSYS D913
CUT SET * 4 C8S18BYP D912
CUT SET * 5 C8S18BYP D913
CUT SET * 6 D812 D912
CUT SET * 7 D812 D913
CUT SET * 8 D913 D912
CUT SET * 9 D913 D913
CUT SET * 10 C8S16BYP D912
CUT SET * 11 C8S16BYP D913
CUT SET * 12 D911 D912
CUT SET * 13 D911 D913
CUT SET * 14 C9LNI0NC C8LCRSYS
CUT SET * 15 C9LNI0NC C8S18BYP
CUT SET * 16 C9LNI0NC D812
CUT SET * 17 C9LNI0NC D913
CUT SET * 18 C9LNI0NC C8S16BYP
CUT SET * 19 C9LNI0NC D911
CUT SET * 20 D911 C8LCRSYS

```

Run 5 (Contd.)

CUT SET * 21	D911	C8S18YF5	CUT SET * 100	C3PE84-1	D804
CUT SET * 22	D911	D812	CUT SET * 101	C3PE84-1	D803
CUT SET * 23	D911	D813	CUT SET * 102	D203	D912
CUT SET * 24	D911	C8S16BY	CUT SET * 103	D203	D913
CUT SET * 25	D911	D811	CUT SET * 104	D203	C9LN10NC
CUT SET * 26	C10LNPPR	C8LCRSYS	CUT SET * 105	D203	D911
CUT SET * 27	C10LNPPR	C8S18YF5	CUT SET * 106	D203	D902
CUT SET * 28	C10LNPPR	D812	CUT SET * 107	D203	C10LNPPR
CUT SET * 29	C10LNPPR	D813	CUT SET * 108	D203	D806
CUT SET * 30	C10LNPPR	C8S16BY	CUT SET * 109	D203	C8S15BY
CUT SET * 31	C10LNPPR	D811	CUT SET * 110	D203	D805
CUT SET * 32	C8PERREC	D912	CUT SET * 111	D202	D804
CUT SET * 33	C8PERREC	D913	CUT SET * 112	D203	D803
CUT SET * 34	C8PERREC	C9LN10NC	CUT SET * 113	D203	D802
CUT SET * 35	C8PERREC	D911	CUT SET * 114	D203	D800
CUT SET * 36	C8PERREC	C10LNPPR	CUT SET * 115	D203	D801
CUT SET * 37	C8S1PERR	D912	CUT SET * 116	D202	D912
CUT SET * 38	C8S1PERR	D913	CUT SET * 117	D202	D913
CUT SET * 39	C8S1PERR	C9LN10NC	CUT SET * 118	D202	C9LN10NC
CUT SET * 40	C8S1PERR	D911	CUT SET * 119	D202	D911
CUT SET * 41	C8S1PERR	C10LNPPR	CUT SET * 120	D202	D902
CUT SET * 42	D810	D912	CUT SET * 121	D202	C10LNPPR
CUT SET * 43	D810	D913	CUT SET * 122	D202	D806
CUT SET * 44	D810	C9LN10NC	CUT SET * 123	D202	C8S15BY
CUT SET * 45	D810	D911	CUT SET * 124	D202	D805
CUT SET * 46	D810	C10LNPPR	CUT SET * 125	D202	D804
CUT SET * 47	D806	C8LCRSYS	CUT SET * 126	D202	D803
CUT SET * 48	D806	C8S18YF5	CUT SET * 127	D202	D792
CUT SET * 49	D806	D812	CUT SET * 128	D202	D900
CUT SET * 50	D806	D813	CUT SET * 129	D202	D801
CUT SET * 51	D806	C8S16BY	CUT SET * 130	D201	D912
CUT SET * 52	D806	D811	CUT SET * 131	D201	D913
CUT SET * 53	D806	C8PERREC	CUT SET * 132	D201	C9LN10NC
CUT SET * 54	D806	C8S1PERR	CUT SET * 133	D201	D911
CUT SET * 55	D806	D810	CUT SET * 134	D201	D902
CUT SET * 56	C8S15BY	C8LCRSYS	CUT SET * 135	D201	C10LNPPR
CUT SET * 57	C8S15BY	C8S18YF5	CUT SET * 136	D201	D906
CUT SET * 58	C8S15BY	D812	CUT SET * 137	D201	C8S15BY
CUT SET * 59	C8S15BY	D813	CUT SET * 138	D201	D905
CUT SET * 60	C8S15BY	C8S16BY	CUT SET * 139	D201	D804
CUT SET * 61	C8S15BY	D811	CUT SET * 140	D201	D803
CUT SET * 62	C8S15BY	C8PERREC	CUT SET * 141	D201	D802
CUT SET * 63	C8S15BY	C8S1PERR	CUT SET * 142	D201	D800
CUT SET * 64	C8S15BY	D810	CUT SET * 143	D201	D801
CUT SET * 65	D805	C8LCRSYS	CUT SET * 144	C2RE62-1	D912
CUT SET * 66	D805	C8S18YF5	CUT SET * 145	C2RE62-1	D913
CUT SET * 67	D805	D812	CUT SET * 146	C2RE62-1	C9LN10NC
CUT SET * 68	D805	D813	CUT SET * 147	C2RE62-1	D911
CUT SET * 69	D805	C8S16BY	CUT SET * 148	C2RE62-1	D902
CUT SET * 70	D805	D811	CUT SET * 149	C2RE62-1	C10LNPPR
CUT SET * 71	D805	C8PERREC	CUT SET * 150	C2RE62-1	D806
CUT SET * 72	D805	C8S1PERR	CUT SET * 151	C2RE62-1	C8S15BY
CUT SET * 73	D805	D810	CUT SET * 152	C2RE62-1	D805
CUT SET * 74	D804	C8LCRSYS	CUT SET * 153	C2RE62-1	D804
CUT SET * 75	D804	C8S18YF5	CUT SET * 154	C2RE62-1	D803
CUT SET * 76	D804	D812	CUT SET * 155	C2RE62-1	D802
CUT SET * 77	D804	D813	CUT SET * 156	C2RE62-1	D801
CUT SET * 78	D804	C8S16BY	CUT SET * 157	C2RE62-1	D800
CUT SET * 79	D804	D811	CUT SET * 158	C2RE62-2	D912
CUT SET * 80	D804	C8PERREC	CUT SET * 159	C2RE62-2	D913
CUT SET * 81	D804	C8S1PERR	CUT SET * 160	C2RE62-2	C9LN10NC
CUT SET * 82	D804	D810	CUT SET * 161	C2RE62-2	D911
CUT SET * 83	D803	C8LCRSYS	CUT SET * 162	C2RE62-2	D902
CUT SET * 84	D803	C8S18YF5	CUT SET * 163	C2RE62-2	C10LNPPR
CUT SET * 85	D803	D812	CUT SET * 164	C2RE62-2	D806
CUT SET * 86	D803	D813	CUT SET * 165	C2RE62-2	C8S15BY
CUT SET * 87	D803	C8S16BY	CUT SET * 166	C2RE62-2	D805
CUT SET * 88	D803	D811	CUT SET * 167	C2RE62-2	D804
CUT SET * 89	D803	C8PERREC	CUT SET * 168	C2RE62-2	D803
CUT SET * 90	D803	C8S1PERR	CUT SET * 169	C2RE62-2	D802
CUT SET * 91	D803	D810	CUT SET * 170	C2RE62-2	D800
CUT SET * 92	C3PE84-1	D912	CUT SET * 171	C2RE62-2	D801
CUT SET * 93	C3PE84-1	D913	CUT SET * 172	D200	D912
CUT SET * 94	C3PE84-1	C9LN10NC	CUT SET * 173	D200	D913
CUT SET * 95	C3PE84-1	D911	CUT SET * 174	D200	C9LN10NC
CUT SET * 96	C3PE84-1	C10LNPPR	CUT SET * 175	D200	D911
CUT SET * 97	C3PE84-1	D806	CUT SET * 176	D200	D902
CUT SET * 98	C3PE84-1	C8S15BY	CUT SET * 177	D200	C10LNPPR
CUT SET * 99	C3PE84-1	D805			

Run 5 (Contd.)

CUT SET • 176 D200 D805
 CUT SET • 179 D200 C8S15BYP
 CUT SET • 180 D200 D805
 CUT SET • 181 D200 D800
 CUT SET • 182 D200 D803
 CUT SET • 183 D200 D802
 CUT SET • 184 D200 D800
 CUT SET • 185 D200 D801

***** END OF CRITICAL PATHS *****

CRITICAL COMPS FOUND IN PATHS

D912 D913 C9LCRYS
 C8PERREC C8S1PERR D810
 D203 D202 D201
 C8S18YPS D812 D813
 D895 C8S15BYP D805
 C2RE62-1 C2RE62-2 D200
 C8S15BYP D911 C9LN10NC
 D804 D803 D802
 D109 C810NPPR
 D209 D911 C8RE84-1
 D911

Run 6

1

MINIMAL CUT SETS FOUND BY COMO FOR LPTP FAULT TREE SAFETY ANALYSIS

CUT SET • 1 D913
 CUT SET • 2 D913
 CUT SET • 3 C9LN10NC
 CUT SET • 4 D911
 CUT SET • 5 C10LNPPR
 CUT SET • 6 D100
 CUT SET • 7 D806 D813
 CUT SET • 8 D806 C8S15BYP
 CUT SET • 9 D806 D811
 CUT SET • 10 D806 C8S18YPS
 CUT SET • 11 D806 D814
 CUT SET • 12 D806 C8PERREC
 CUT SET • 13 D806 C8S1PERR
 CUT SET • 14 D806 D810
 CUT SET • 15 C8S15BYP D913
 CUT SET • 16 C8S15BYP C8S16BYP
 CUT SET • 17 C8S15BYP D811
 CUT SET • 18 C8S15BYP C8S18YPS
 CUT SET • 19 C8S15BYP D814
 CUT SET • 20 C8S15BYP C8PERREC
 CUT SET • 21 C8S15BYP C8S1PERR
 CUT SET • 22 C8S15BYP D810
 CUT SET • 23 D805 D813
 CUT SET • 24 D805 C8S15BYP
 CUT SET • 25 D805 D911
 CUT SET • 26 D805 C8S18YPS
 CUT SET • 27 D805 D814
 CUT SET • 28 D805 C8PERREC
 CUT SET • 29 D805 C8S1PERR
 CUT SET • 30 D805 D810
 CUT SET • 31 D804 D813
 CUT SET • 32 D804 C8S15BYP
 CUT SET • 33 D804 D811
 CUT SET • 34 D804 C8S18YPS
 CUT SET • 35 D804 D914
 CUT SET • 36 D804 C8PERREC
 CUT SET • 37 D804 C8S1PERR
 CUT SET • 38 D804 D810
 CUT SET • 39 D803 D813
 CUT SET • 40 D803 C8S15BYP
 CUT SET • 41 D803 D911
 CUT SET • 42 D803 C8S18YPS
 CUT SET • 43 D803 D814
 CUT SET • 44 D803 C8PERREC
 CUT SET • 45 D803 C8S1PERR
 CUT SET • 46 D803 D810
 CUT SET • 47 C3RE84-1 D804
 CUT SET • 48 C3RE84-1 C8S15BYP
 CUT SET • 49 C3RE84-1 D805
 CUT SET • 50 C3RE84-1 D804
 CUT SET • 51 C3RE84-1 D803
 CUT SET • 52 D802

CUT SET • 53 D203 D806
 CUT SET • 54 D203 C8S15BYP
 CUT SET • 55 D203 D805
 CUT SET • 56 D203 D804
 CUT SET • 57 D203 D803
 CUT SET • 58 D203 D802
 CUT SET • 59 D203 D800
 CUT SET • 60 D203 D801
 CUT SET • 61 D202 D805
 CUT SET • 62 D202 D804
 CUT SET • 63 D202 C8S15BYP
 CUT SET • 64 D202 D805
 CUT SET • 65 D202 D804
 CUT SET • 66 D202 D803
 CUT SET • 67 D202 D802
 CUT SET • 68 D202 D800
 CUT SET • 69 D202 D801
 CUT SET • 70 D201 D806
 CUT SET • 71 D201 D805
 CUT SET • 72 D201 C8S15BYP
 CUT SET • 73 D201 D805
 CUT SET • 74 D201 D804
 CUT SET • 75 D201 D803
 CUT SET • 76 D201 D802
 CUT SET • 77 D201 D800
 CUT SET • 78 D201 D801
 CUT SET • 79 C2RE62-1 D806
 CUT SET • 80 C2RE62-1 C8S15BYP
 CUT SET • 81 C2RE62-1 D805
 CUT SET • 82 C2RE62-1 D804
 CUT SET • 83 C2RE62-1 D803
 CUT SET • 84 C2RE62-1 D802
 CUT SET • 85 C2RE62-1 D800
 CUT SET • 86 C2RE62-1 D801
 CUT SET • 87 C2RE62-1 D800
 CUT SET • 88 C2RE62-2 D806
 CUT SET • 89 C2RE62-2 D805
 CUT SET • 90 C2RE62-2 C8S15BYP
 CUT SET • 91 C2RE62-2 D804
 CUT SET • 92 C2RE62-2 D803
 CUT SET • 93 C2RE62-2 D802
 CUT SET • 94 C2RE62-2 D800
 CUT SET • 95 C2RE62-2 D801
 CUT SET • 96 D809
 CUT SET • 97 D808
 CUT SET • 98 D200 D806
 CUT SET • 99 D200 C8S15BYP
 CUT SET • 100 D200 D805
 CUT SET • 101 D200 D804
 CUT SET • 102 D200 D803
 CUT SET • 103 D200 D802
 CUT SET • 104 D200 D800

Run 6 (Contd.)

CUT SET # 105	D203	D801	D202	D201	C2RE52-1	C2RE52-2	D200
END OF CRITICAL PATHS			CSLNIDNC	D911	D702	C18L4PPR	C8S18VPS
			D804	D803	D802	D809	D801
			D100	D914	C8PE7SEC	C8PE84-1	D805

CRITICAL CC:PS FOUND IN PATHS

D912	D913	D913	C8S15BYP	D811
C8S1PERR	D910	D805	C8S15BYP	D805

Runs 15, 16

1
 MINIMAL CUT SETS FOUND BY COMBO FOR LPTR FAULT TREE SAFETY ANALYSIS
 CUT SET # 1 D702
 CUT SET # 2 D100
 END OF CRITICAL PATHS

1
 CRITICAL COMPONENTS FOUND IN PATHS

D702 D100

INPUT DECKS SHOWING WHICH COMPONENTS AND HOUSES WERE TURNED ON

Run 1

/ RATES					
H101	0.0	0.0	H203	0.0	1.0
H202	0.0	0.0	H207	0.0	1.0
H205	0.0	1.0	H206	0.0	0.0
H301	0.0	0.0	H302	0.0	1.0
H303	0.0	0.0	H304	0.0	1.0
H305	0.0	0.0	H306	0.0	1.0
H307	0.0	0.0	H308	0.0	1.0
H401	0.0	0.0	H402	0.0	1.0
H403	0.0	1.0	H404	0.0	0.0
H405	0.0	1.0	H406	0.0	0.0
H407	0.0	1.0	H408	0.0	0.0
H501	0.0	1.0	H502	0.0	0.0
H503	0.0	1.0	H504	0.0	0.0
H505	0.0	1.0	H506	0.0	0.0
H509	0.0	0.0	H507	0.0	1.0
H510	0.0	0.0	H511	0.0	1.0
H602	0.0	1.0	H603	0.0	0.0
H604	0.0	1.0	H605	0.0	0.0
H606	0.0	1.0	H607	0.0	0.0
H701	0.0	0.0	H703	0.0	1.0
H702	0.0	1.0	H704	0.0	0.0
H800	0.0	0.0	H801	0.0	1.0
H1001	0.0	1.0	H1003	0.0	0.0
H1002	0.0	0.0	H1005	0.0	1.0
H1006	0.0	0.0	H1007	0.0	1.0
H508	0.0	1.0	H601	0.0	1.0
H705	0.0	1.0	H706	0.0	1.0
H707	0.0	1.0	H708	0.0	1.0
H1004	0.0	1.0	H1008	0.0	1.0
END					

Run 2

/ RATES					
H101	0.0	0.0	H203	0.0	1.0
H202	0.0	0.0	H207	0.0	1.0
H205	0.0	1.0	H206	0.0	0.0
H301	0.0	0.0	H302	0.0	1.0
H303	0.0	0.0	H304	0.0	1.0
H305	0.0	0.0	H306	0.0	1.0
H307	0.0	0.0	H308	0.0	1.0
H401	0.0	0.0	H402	0.0	1.0
H403	0.0	1.0	H404	0.0	0.0
H405	0.0	1.0	H406	0.0	0.0
H407	0.0	1.0	H408	0.0	0.0
H501	0.0	1.0	H502	0.0	0.0
H503	0.0	1.0	H504	0.0	0.0
H505	0.0	1.0	H506	0.0	0.0
H509	0.0	0.0	H507	0.0	1.0
H510	0.0	0.0	H511	0.0	1.0
H602	0.0	1.0	H603	0.0	0.0
H604	0.0	1.0	H605	0.0	0.0
H606	0.0	1.0	H607	0.0	0.0

Run 2 (Contd.)

H701	0.0	0.0	H703	0.0	1.0
H702	0.0	1.0	H704	0.0	0.0
H800	0.0	0.0	H801	0.0	1.0
H1001	0.0	1.0	H1003	0.0	0.0
H1002	0.0	0.0	H1005	0.0	1.0
H1006	0.0	0.0	H1007	0.0	1.0
H508	0.0	1.0	H501	0.0	1.0
H705	0.0	1.0	H706	0.0	1.0
H707	0.0	1.0	H708	0.0	1.0
H1004	0.0	1.0	C9LN10NC	0.0	1.0

END

Run 3

POWER EXCEEDS SIX MEGAWATTS

RATES					
H101	0.0	0.0	H203	0.0	1.0
H202	0.0	0.0	H207	0.0	1.0
H205	0.0	1.0	H206	0.0	0.0
H301	0.0	1.0	H302	0.0	0.0
H303	0.0	1.0	H304	0.0	0.0
H305	0.0	0.0	H306	0.0	1.0
H307	0.0	0.0	H308	0.0	1.0
H401	0.0	0.0	H402	0.0	1.0
H403	0.0	1.0	H404	0.0	0.0
H405	0.0	1.0	H406	0.0	0.0
H407	0.0	1.0	H408	0.0	0.0
H501	0.0	1.0	H502	0.0	0.0
H503	0.0	1.0	H504	0.0	0.0
H505	0.0	1.0	H506	0.0	0.0
H509	0.0	0.0	H507	0.0	1.0
H510	0.0	0.0	H511	0.0	1.0
H602	0.0	1.0	H603	0.0	0.0
H604	0.0	1.0	H605	0.0	0.0
H606	0.0	1.0	H607	0.0	0.0
H701	0.0	1.0	H703	0.0	0.0
H702	0.0	1.0	H704	0.0	0.0
H700	0.0	0.0	H801	0.0	1.0
H1001	0.0	0.0	H1003	0.0	1.0
H1002	0.0	0.0	H1005	0.0	1.0
H1006	0.0	0.0	H1007	0.0	1.0
H508	0.0	1.0	H501	0.0	1.0
H705	0.0	1.0	H706	0.0	1.0
H707	0.0	1.0	H708	0.0	1.0
H1004	0.0	1.0			

END

Run 4

POWER REACHES 4.5 MEGAWATTS

/ RATES

H101	0.0	0.0	H203	0.0	1.0
H202	0.0	1.0	H207	0.0	0.0
H205	0.0	1.0	H208	0.0	0.0
H301	0.0	1.0	H302	0.0	0.0
H303	0.0	1.0	H304	0.0	0.0
H305	0.0	0.0	H306	0.0	1.0
H307	0.0	0.0	H308	0.0	1.0
H401	0.0	0.0	H402	0.0	1.0
H403	0.0	1.0	H404	0.0	0.0
H405	0.0	1.0	H406	0.0	0.0
H407	0.0	1.0	H408	0.0	0.0
H501	0.0	1.0	H502	0.0	0.0
H503	0.0	1.0	H504	0.0	0.0
H505	0.0	1.0	H506	0.0	0.0
H509	0.0	0.0	H507	0.0	1.0
H510	0.0	0.0	H511	0.0	1.0
H502	0.0	1.0	H603	0.0	0.0
H604	0.0	1.0	H605	0.0	0.0
H606	0.0	1.0	H607	0.0	0.0
H701	0.0	1.0	H703	0.0	0.0
H702	0.0	1.0	H704	0.0	0.0
H800	0.0	0.0	H801	0.0	1.0
H1001	0.0	1.0	H1003	0.0	0.0
H1002	0.0	0.0	H1005	0.0	1.0
H1006	0.0	0.0	H1007	0.0	1.0
H508	0.0	1.0	H601	0.0	1.0
H705	0.0	1.0	H706	0.0	1.0
H707	0.0	1.0	H708	0.0	1.0
H1004	0.0	1.0			
END					

Run 5

FAST PERIOD SCRAM LOW POWER

/ RATES

H101	0.0	0.0	H203	0.0	0.0
H202	0.0	1.0	H207	0.0	0.0
H205	0.0	1.0	H208	0.0	0.0
H301	0.0	0.0	H302	0.0	1.0
H303	0.0	0.0	H304	0.0	1.0
H305	0.0	1.0	H306	0.0	0.0
H307	0.0	1.0	H308	0.0	0.0
H401	0.0	1.0	H402	0.0	0.0
H403	0.0	1.0	H404	0.0	0.0
H405	0.0	1.0	H406	0.0	0.0
H407	0.0	1.0	H408	0.0	0.0
H501	0.0	1.0	H502	0.0	0.0
H503	0.0	1.0	H504	0.0	0.0
H505	0.0	1.0	H506	0.0	0.0
H509	0.0	0.0	H507	0.0	1.0
H510	0.0	0.0	H511	0.0	1.0
H602	0.0	1.0	H603	0.0	0.0
H604	0.0	1.0	H605	0.0	0.0
H606	0.0	1.0	H607	0.0	0.0
H701	0.0	0.0	H703	0.0	1.0
H702	0.0	0.0	H704	0.0	1.0
H800	0.0	1.0	H801	0.0	0.0
H1001	0.0	1.0	H1003	0.0	0.0
H1002	0.0	1.0	H1005	0.0	0.0
H1006	0.0	1.0	H1007	0.0	0.0
H508	0.0	1.0	H601	0.0	1.0
H705	0.0	1.0	H706	0.0	1.0
H707	0.0	1.0	H708	0.0	1.0
H1004	0.0	1.0			
END					

Run 6

	FAST PERIOD		HIGH POWER	
RATES				
H101	0.0	0.0	H203	0.0
H102	0.0	1.0	H207	0.0
H105	0.0	1.0	H206	0.0
H301	0.0	0.0	H302	0.0
H303	0.0	0.0	H304	0.0
H305	0.0	1.0	H306	0.0
H307	0.0	1.0	H308	0.0
H401	0.0	1.0	H402	0.0
H403	0.0	1.0	H404	0.0
H405	0.0	1.0	H406	0.0
H407	0.0	1.0	H408	0.0
H501	0.0	1.0	H502	0.0
H503	0.0	1.0	H504	0.0
H505	0.0	1.0	H506	0.0
H509	0.0	0.0	H507	0.0
H510	0.0	0.0	H511	0.0
H602	0.0	1.0	H603	0.0
H604	0.0	1.0	H605	0.0
H606	0.0	1.0	H607	0.0
H701	0.0	0.0	H703	0.0
H702	0.0	0.0	H704	0.0
H800	0.0	0.0	H801	0.0
H1001	0.0	1.0	H1003	0.0
H1002	0.0	0.0	H1005	0.0
H1006	0.0	1.0	H1007	0.0
H508	0.0	1.0	H601	0.0
H705	0.0	1.0	H706	0.0
H707	0.0	1.0	H708	0.0
H1004	0.0	1.0		
END				

Run 15

STARTUP ACCIDENT--SLOW SCRAMS AND PERIOD FAILED--POWER>3MW				
RATES				
H101	0.0	0.0	H203	0.0
H202	0.0	1.0	H207	0.0
H205	0.0	1.0	H206	0.0
H301	0.0	1.0	H302	0.0
H303	0.0	1.0	H304	0.0
H305	0.0	1.0	H306	0.0
H307	0.0	1.0	H308	0.0
H401	0.0	1.0	H402	0.0
H403	0.0	1.0	H404	0.0
H405	0.0	1.0	H406	0.0
H407	0.0	1.0	H408	0.0
H501	0.0	1.0	H502	0.0
H503	0.0	1.0	H504	0.0
H505	0.0	1.0	H506	0.0
H509	0.0	0.0	H507	0.0
H510	0.0	0.0	H511	0.0
H602	0.0	1.0	H603	0.0
H604	0.0	1.0	H605	0.0
H606	0.0	1.0	H607	0.0
H701	0.0	1.0	H703	0.0
H702	0.0	1.0	H704	0.0
H800	0.0	0.0	H801	0.0
H1001	0.0	1.0	H1003	0.0
H1002	0.0	0.0	H1005	0.0
H1006	0.0	1.0	H1007	0.0
H508	0.0	1.0	H601	0.0
H705	0.0	1.0	H706	0.0
H707	0.0	1.0	H708	0.0
H1004	0.0	1.0		
END				

Run 16

STARTUP ACCIDENT--FAIL D200 AND COLN10NC
/ PATES

D200	0.0	1.0	COLN10NC	0.0	1.0
H101	0.0	0.0	H203	0.0	1.0
H202	0.0	0.0	H207	0.0	1.0
H209	0.0	1.0	H206	0.0	0.0
H301	0.0	0.0	H302	0.0	1.0
H303	0.0	0.0	H304	0.0	1.0
H305	0.0	0.0	H306	0.0	1.0
H307	0.0	0.0	H308	0.0	1.0
H401	0.0	0.0	H402	0.0	1.0
H403	0.0	1.0	H404	0.0	0.0
H405	0.0	1.0	H406	0.0	0.0
H407	0.0	1.0	H408	0.0	0.0
H501	0.0	1.0	H502	0.0	0.0
H503	0.0	1.0	H504	0.0	0.0
H505	0.0	1.0	H506	0.0	0.0
H509	0.0	0.0	H507	0.0	1.0
H510	0.0	0.0	H511	0.0	1.0
H602	0.0	1.0	H603	0.0	0.0
H604	0.0	1.0	H605	0.0	0.0
H606	0.0	1.0	H607	0.0	0.0
H701	0.0	0.0	H703	0.0	1.0
H702	0.0	1.0	H704	0.0	0.0
H800	0.0	0.0	H801	0.0	1.0
H1001	0.0	1.0	H1003	0.0	0.0
H1002	0.0	0.0	H1005	0.0	1.0
H1006	0.0	0.0	H1007	0.0	1.0
H508	0.0	1.0	H601	0.0	1.0
H705	0.0	1.0	H706	0.0	1.0
H707	0.0	1.0	H708	0.0	1.0
H1004	0.0	1.0			
END					

INPUT DECK REPRESENTING THE "AND" AND "OR" GATES FOUND IN THE FAULT TREE

*TREBIL FAULT TREE BUILDING PROGRAM

LPTR FAULT TREE SAFETY ANALYSIS
NUMBER OF GATES, IG----- 230
COMBO STARTING VALUE, MIN----- 1
COMBO ENDING VALUE, MAX----- 2
CUT SET - PATH SET SWITCH, IDEX1----- 0
PRINT - PUNCH SWITCH, IDEX2----- 0
MONTE CARLO STARTER, ICS----- 0
NO. OF RANDOM NUMBERS TO REJECT, NREJEC----- 0
NO. OF MONTE CARLO TRIALS, NTR----- 0
MIXING PARAMETER SWITCH, IREN----- 0
MONTE CARLO MIXING PARAMETER, TAR----- 0.

*TREBIL FAULT TREE BUILDING PROGRAM

LPTR FAULT TREE SAFETY ANALYSIS
NAME TYPE INPUTS-----
TOP OR 2 1 G101 G102 D100
G101 AND 3 0 G105A G105B G103
G102 AND 3 0 G104 G105C G105D
G103 OR 2 0 G105C G105D
G104 OR 2 0 G105A G105B
G105A OR 1 1 G106A D101A
G105B OR 1 1 G106B D101B
G105C OR 1 1 G106C D101C
G105D OR 1 1 G106D D101D
G106A OR 1 1 G107A D102A
G106B OR 1 1 G107B D102B
G106C OR 1 1 G107C D102C
G106D OR 1 1 G107D D102D
G107A AND 2 0 G108A G109A
G107B AND 2 0 G108B G109B
G107C AND 2 0 G108C G109C
G107D AND 2 0 G108D G109D
G108A OR 1 1 G200A D103A
G108B OR 1 1 G200B D103B
G108C OR 1 1 G200C D103C
G108D OR 1 1 G200D D103D
G109A OR 1 1 G700A H101
G109B OR 1 1 G700B H101
G109C OR 1 1 G700C H101
G109D OR 1 1 G700D H101
G200A OR 1 1 G201 D200
G200B OR 1 1 G201 D200
G200C OR 1 1 G201 D200
G200D OR 1 1 G201 D200
G201 OR 1 2 G203 C2RE62-1 D201
G203 OR 2 1 G204 G205
G204 AND 2 0 G206 G212
G205 AND 2 0 G206 G210
G206 OR 1 1 G207 D202
G207 AND 2 0 G208 G209
G208 OR 1 1 G300 D203
G209 OR 1 1 G215 H202
G210 AND 1 1 G211 H203
G211 OR 0 2 D204 C2S2-1
G212 OR 1 1 G213 H205
G213 AND 1 1 G214 H206
G214 OR 0 2 C2PCLF C2RE75-1
G215 AND 1 1 G216 H207

G216	OR	1	1	G1000	C2RE03-1
G300	AND	2	0	G301	G317
G301	OR	1	1	G302	D300
G302	AND	2	0	G303	G314
G303	OR	1	1	G304	D301
G304	AND	2	0	G305	G311
G305	OR	1	1	G306	D302
G306	AND	2	0	G307	G308
G307	OR	1	1	G400	D303
G308	OR	1	1	G309	H307
G309	AND	1	1	G310	H308
G310	OR	1	1	G311	C3PE01-2
G311	OR	1	1	G312	H305
G312	AND	1	1	G313	H306
G313	OR	1	1	G314	C3PE02-2
G314	OR	1	1	G315	H303
G315	AND	1	1	G316	H304
G316	OR	1	1	G317	C3PE03-1
G317	OR	1	1	G318	H301
G318	AND	1	1	G319	H302
G319	OR	1	1	G401	C3RE04-1
G400	AND	2	0	G402	G417
G401	OR	1	1	G403	D400
G402	AND	2	0	G404	G414
G403	OR	1	1	G405	D401
G404	AND	2	0	G406	G411
G405	OR	1	1	G407	D402
G406	AND	2	0	G408	G408
G407	OR	1	1	G409	D403
G408	OR	1	1	G410	H407
G409	AND	1	1	G411	H408
G410	OR	0	2	C4TROBLC	C4PE10-2
G411	OR	1	1	G412	H405
G412	AND	1	1	G413	H406
G413	OR	0	2	C4TROBLD	C4PE19-2
G414	OR	1	1	G415	H403
G415	AND	1	1	G416	H404
G416	OR	0	3	C4EXSCRM	C4C01L32 C4RE32-1
G417	OR	1	1	G418	H401
G418	AND	1	1	G419	H402
G419	OR	1	1	G1100	C4RE00-2
G500	AND	2	0	G501	G518
G501	OR	1	1	G502	D500
G502	AND	2	0	G503	G515
G503	OR	1	1	G504	G501
G504	AND	2	0	G505	G512
G505	OR	2	1	G506	G508
G506	AND	1	1	G507	H507
G507	OR	1	1	G508	D503
G508	AND	1	1	G509	H500
G509	AND	2	0	G510	G511
G510	OR	0	3	H509	H510
G511	OR	0	2	D504	C5PE07
G512	OR	1	1	G513	H505
G513	AND	1	1	G514	H506
G514	OR	0	4	C5R0T	C5SU2-1
G515	OR	1	1	G516	H503
G516	AND	1	1	G517	H504
G517	OR	0	2	C5TROBLA	C5RE16-2
G518	OR	1	1	G519	H501
G519	AND	1	1	G520	H502
G520	OR	0	2	C5TROBLB	C5RE17-2
G600	AND	2	0	G601	D610
G601	OR	1	1	G602	D601
G602	AND	2	0	G603	G607
G603	OR	1	1	G604	D602
G604	AND	1	1	G605	H601
G605	OR	1	1	G606	H602
G606	OR	1	1	G607	H604
G606	AND	0	2	C6SCRF0B	H603

G608	AND	1	1	G609	H705	
G609	OF	0	3	C610PMS	C601L2	C6R2-1
G610	OF	1	1	G611	H706	
G611	AND	1	1	G612	H707	
G612	OF	0	3	C611LDS	C601L2	C6R2-1
G700A	OF	1	2	G701A	C7001LA	D701A
G700B	OF	1	2	G701B	C7001LB	D701B
G700C	OF	1	2	G701C	C7001LC	D701C
G700D	OF	1	2	G701D	C7001LD	D701D
G701A	OF	3	0	G702A	G703A	G704A
G701B	OF	3	0	G702B	G703B	G704B
G701C	OF	3	0	G702C	G703C	G704C
G701D	OF	3	0	G702D	G703D	G704D
G702A	AND	1	2	G705A	H701	H702
G702B	AND	1	2	G705B	H701	H702
G702C	AND	1	2	G705C	H701	H702
G702D	AND	1	2	G705D	H701	H702
G703A	AND	1	2	G706A	H702	H703
G703B	AND	1	2	G706B	H702	H703
G703C	AND	1	2	G706C	H702	H703
G703D	AND	1	2	G706D	H702	H703
G704A	AND	1	2	G707A	H703	H704
G704B	AND	1	2	G707B	H703	H704
G704C	AND	1	2	G707C	H703	H704
G704D	AND	1	2	G707D	H703	H704
G705A	OF	1	2	G708	C7001PA	D702
G705B	OF	1	2	G708	C7001PB	D702
G705C	OF	1	2	G708	C7001PC	D702
G705D	OF	1	2	G708	C7001PD	D702
G706A	OF	1	2	G709	C7001PA	D702
G706B	OF	1	2	G709	C7001PB	D702
G706C	OF	1	2	G709	C7001PC	D702
G706D	OF	1	2	G709	C7001PD	D702
G707A	OF	1	2	G710	C7001PA	D702
G707B	OF	1	2	G710	C7001PB	D702
G707C	OF	1	2	G710	C7001PC	D702
G707D	OF	1	2	G710	C7001PD	D702
G708	AND	3	1	G711	G715	G719
G709	AND	4	0	G711	G715	G719
G710	AND	1	3	G800	H706	H707
G711	OF	1	2	G712	D703	D704
G712	OF	1	1	G713	D705	
G713	OF	1	1	G714	D706	
G714	OF	0	2	C710NCHA	D707	
G715	OF	1	2	G716	D709	D710
G716	OF	1	1	G717	D711	
G717	OF	1	1	G718	D712	
G718	OF	0	2	C710NCHB	D713	
G719	OF	1	2	G720	D715	D716
G720	OF	1	1	G721	D717	
G721	OF	1	1	G722	D718	
G722	OF	0	2	C710NCHC	D719	
G800	OF	1	2	G801	D800	D801
G801	OF	1	1	G802	D802	
G802	OF	1	1	G803	D803	
G803	OF	1	1	G804	D804	
G804	OF	1	2	G805	C8518YP	D805
G805	OF	1	1	G81019	D806	
G806	OF	1	1	G807	D807	
G807	OF	1	1	G808	C8R24-1	
G808	OF	1	1	G809	D809	
G809	OF	1	1	G810	C8518YP	
G810	OF	1	1	G811	D809	
G811	OF	2	1	G812	G813	D810
G812	OF	0	2	C8518YP	D811	
G813	OF	1	1	G814	C8518YP	
G814	OF	1	1	G815	C8518YP	
G815	OF	2	0	G816	G816	
G816	AND	1	1	G817	H800	
G817	OF	0	4	C8518YP5	C8518YP5	D812
G818	AND	1	1	G819	H801	D813
G819	OF	1	3	G81019	C8518YP5	D813
G900	OF	1	1	G901	D901	D814

G901	OP	1	1	G902	C90L2-1
G902	OP	1	1	G903	L90L
G903	OP	1	1	G904	C90LCC
G904	OP	1	1	G917	D903
G905	OP	1	1	G906	D904
G906	OP	1	1	G907	C90L23-1
G907	OP	1	1	G908	D905
G908	OP	1	1	G909	C90LCC
G909	OP	1	1	G911	D906
G910	OP	1	2	G911	C90LPEC D914
G911	OP	1	1	G912	D907
G912	OP	1	1	G913	C90LWATR
G913	OP	1	2	G914	C90L10MC D908
G914	OP	0	2	G915	D910
G915	OP	1	2	G916	C90L10MC D911
G916	OP	0	2	G917	D913
G1000	OR	2	1	G1001	G1002
G1001	AND	2	0	G1003	G1004
G1002	AND	2	0	G1005	G1006
G1003	OP	1	1	G1007	H1001
G1004	OP	1	1	G1008	D1001
G1005	OR	1	1	G1009	D1002
G1006	OP	1	1	G1010	H1002
G1007	AND	1	1	G1011	H1003
G1008	AND	1	1	G1012	H1004
G1009	AND	2	0	G1012	G1013
G1010	AND	1	1	G1013	H1005
G1011	OR	1	1	G1015	C1053PLR
G1012	OP	1	1	G1016	D1003
G1013	OP	1	3	G1021	C10P86C0 D1004
G1014	OR	1	1	G1015	C1053LNR
G1015	OP	1	1	G1017	C10LOGNR
G1016	OP	1	1	G1018	H1006
G1017	OR	1	1	G1019	D1007
G1018	AND	1	1	G1020	H1007
G1019	OR	1	1	G915	C10LNPPR
G1020	OR	1	1	G910	C10S2LLR
G1021	OR	1	1	G1022	D1005
G1022	OR	0	2	C10514	D1006
G1100	OR	1	1	G1101	D1101
G1101	OR	1	1	G1102	C11R21-1
G1102	OR	1	1	G1103	D1102
G1103	OR	1	1	G1104	C11SLCA
G1104	OP	1	1	G713	D1103
END		-8-8			